Model Predictive Direct Current Control of Modular Multi-Level Converters

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***Abstract*—Modular Multi-level Converters (M2LCs) are mostly controlled by using a hierarchical control scheme, where at least two control loops are required for controlling the load currents and balancing the capacitor voltages. This paper proposes a single controller, which is based on Model Predictive Direct Current Control (MPDCC) with long prediction horizons, to directly control the load currents within tight bounds around their sinusoidal references and balance the capacitor voltages. MPDCC uses a model of the converter for an online optimization process to deliver the best possible performance during both steady-state and transient operating conditions. A conceptual description and control algorithm of the proposed controller are presented in this paper. To validate the proposed concept, simulated performance of a three-phase, three-level 2 MVA grid connected M2LC is presented with a discussion. A comparison with a vector control (VC) pulse width modulation (PWM) scheme is also carried out to demonstrate the improvements in performance associated with the MPDCC scheme.**

I. Introduction

Recently, Modular Multi-level Converter (M2LC) topology, as shown in Fig. 1, has gained popularity in medium to high power applications, because it provides number of advantages over other available multi-level converter topologies, such as Neutral Point Clamped Voltage Source Converter (NPC VSC), Flying Capacitor Voltage Source Converter (FC VSC) and Series Connected H-Bridge Voltage Source Converter (SCHB VSC). Some of the features of M2LC are simple process of scaling the number of output voltage levels by a linear addition of identical modules, capacitor free dc-link, continuous arm currents, reduced voltage rating of the switches and redundant switching operations. These features of the M2LC topology make it suitable for various applications, such as high-voltage direct current (HVDC) transmission [1]–[4], motor drives [5]–[8], traction motors [9], [10], static synchronous compensator (STATCOM) [11], [12] and as a general grid connected converter [1], [6], [9], [10], [13]–[20].

Because of a series connection of module capacitors, a control scheme that drives the M2LC has two primary objectives of minimizing the variations in the capacitor voltages and controlling the three-phase load currents or the output power. Various control schemes, mostly hierarchical, are available to fulfil such objectives [6]–[9], [13], [15], [18], [21]. These schemes employ two control loops, where an upper loop uses a current controller in conjunction with a modulator to control the load currents. A lower loop utilizes the redundancy of the converter switching states to balance the capacitor voltages.

This paper proposes Model Predictive Direct Current Control (MPDCC) [22] with long prediction horizon for controlling

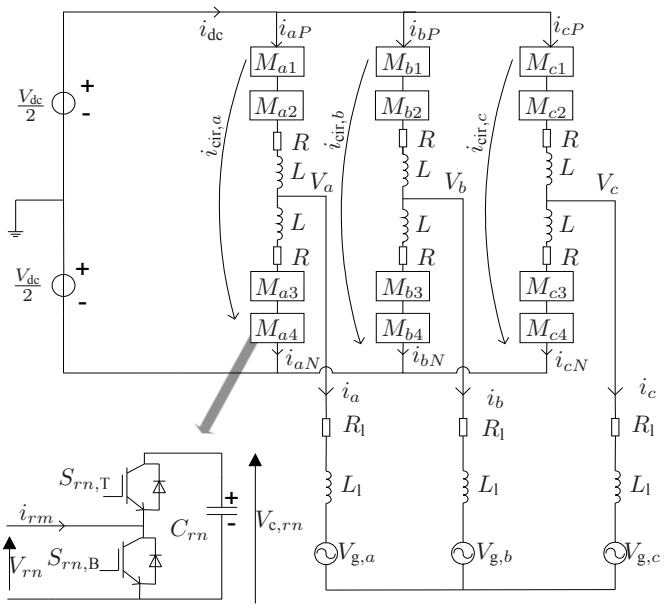

Fig. 1: Modular Multi-level Converter and a module

the M2LC, where the controller directly sets the M2LC switch positions without a modulator. MPDCC has a single control loop to control the load currents and balance the capacitor voltages. In this control scheme, constraints are imposed on the load currents that can be kept within symmetrical bounds around their sinusoidal references. Furthermore, the capacitor voltages can be easily balanced around their nominal voltages and, as a result, components are equally voltage stressed, arm currents or circulating currents are reduced and conduction losses are lowered.

MPDCC has two key benefits. Firstly, at steady-state operating conditions and for a given load current distortion, the lowest possible switching frequency can be achieved by the online optimization process as described in the subsequent sections. Secondly, during transients, fast current response can be achieved and the capacitor voltages can be kept close to their references. The proposed control scheme is verified using MATLAB/SIMULINK simulations. A comparison with a PWM based scheme shows that MPDCC performs better and achieves a very fast current response during power-up and power-down transients.

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II. Modular Multi-level converter

A. Configuration of the M2LC topology

A grid connected three-level M2LC is shown in Fig. 1. Each phase-leg of the converter is divided into two halves, called arms. Each arm consists of $N = 2$ modules, which are represented as M_{rn}, $r \in \{a, b, c\}$, $n \in \{1, 2, 3, 4\}$, a resistor, R, that models conduction losses and an arm inductor, L. A typical module acts like a chopper cell with a capacitor, C_{rn}, which is connected to its terminals as shown in Fig. 1. The individual module has two switching states $u_{rn} \in \{0, 1\}$, where 1 means that the capacitor is connected in the circuit, i.e. switch $S_{rn,T}$ is turned on. The turn on operation of the switches in a module is complementary to one another. The output terminal, V_r, is connected to the load, which consists of an inductor L_l in series with a resistor R_l and a grid voltage $V_{\mathrm{g},r}$. Further details on the operating principle and characteristics of the M2LC can be found in [1], [6], [8]–[10], [13]–[15].

The converter under consideration provides three $(N + 1)$ voltage levels, $\frac{V_{\mathrm{dc}}}{2}$, 0, $\frac{-V_{\mathrm{dc}}}{2}$, at its output terminal with respect to the supply ground. It is also possible to generate $2N + 1$ voltage levels at the output terminals by varying the number of modules inserted in a phase-leg to N, $N - 1$ and $N + 1$ [18], [23]. A control decision to generate $2N + 1$ voltage levels depends on the DC-link voltage, number of modules in an arm and variation in the phase-leg voltage that will appear across the arm inductors. For example, if N is a small number then switching either $N + 1$ or $N - 1$ number of modules in a phase-leg will generate large voltage variations across the arm inductors and arm currents, i_{rm}, $m \in \{P, N\}$, will carry higher order harmonic currents. Thus, it may not be a viable modulation scheme to drive the converter. The scope of the paper is limited to the generation of $N + 1$ voltage levels, but can be easily extended to $2N + 1$ voltage levels.

B. M2LC Model

It is easy to establish that there are five independent currents in the converter, refer Fig. 1 and state equations of the currents can be derived by applying Kirchhoff's voltage law around the five circuit meshes.

The module capacitors are charged or discharged depending on the module's switching state and polarity of the arm current. The state equations of the capacitor voltages can also be easily derived by applying Kirchhoff's current law in a module.

The output equations for the load currents in phases a, b and c are as follows:

$$i_r(t) = i_{rP}(t) - i_{rN}(t),\ r \in \{a, b, c\} \tag{1}$$

The differential equations, which define the circulating currents in phases a, b and c are as follows [16]

$$i_{\mathrm{cir},r}(t) = \frac{i_{rP}}{2}(t) + \frac{i_{rN}}{2}(t) - \frac{i_{\mathrm{dc}}}{3},\ r \in \{a, b, c\} \tag{2}$$

III. Model Predictive Direct Current Control

Model Predictive Direct Current Control (MPDCC), which has its roots in constrained optimal control, has recently been introduced for multi-level converters [22]. MPDCC features an online optimization process to determine the future control inputs, without a modulation stage, to directly control the load currents and also offers a flexibility to handle system objectives. In the MPDCC scheme, an optimal control problem is solved at each sampling instant k, to generate present and future sequence of inputs $\big[\mathbf{u}(k), \mathbf{u}(k{+}1),..., \mathbf{u}(k{+}N_p{-}1)\big]$, by measuring current states and previous inputs of the converter such that the objective (cost) function is minimized. Only the first input $\mathbf{u}(k)$ is applied and the process is repeated at the next sampling instant $k + 1$ in accordance with the so called receding horizon policy [24], [25].

MPDCC, as presented in this paper, is based on an internal prediction model of the M2LC to predict output variables i.e. the arm currents and capacitor voltages over a number of time steps known as *prediction horizon* N_p. The N_p is defined by the bounds set around the load currents. The output variables are predicted by considering a number of switching transitions over the length of N_p and the length is referred to as *switching horizon*, N_s. In this scheme, the load currents are to be kept within specified bounds around the sinusoidal references while balancing the capacitor voltages and minimizing the switching frequency.

A. Internal Prediction Model

The converter is modeled using two linear state-space models to predict the aforementioned variables. The first model predicts the arm currents and its state vector encompasses the arm currents in phases a and b, dc-link current and grid voltages in $\alpha\beta$ domain. The state vector is defined as

$$\mathbf{x_i} = [i_{aP}\ i_{aN}\ i_{bP}\ i_{bN}\ i_{\mathrm{dc}}\ V_{g,\alpha}\ V_{g,\beta}]^T \tag{3}$$

The input vector to the model is the switching states of the modules

$$\mathbf{u} = [u_{a1}\ u_{a2}\ u_{a3}\ \cdots\ u_{c3}\ u_{c4}]^T \in \{0, 1\}^{12} \tag{4}$$

and the load currents constitute the output vector

$$\mathbf{y_i} = [i_a\ i_b\ i_c]^T. \tag{5}$$

In the first model, the capacitor voltages are assumed as parameters within the prediction horizon, N_p. Such an assumption does not compromise the performance of the proposed concept, because over the length of N_p there is a negligible change in the capacitor voltages.

A second model is derived to predict the evolution of the capacitor voltages for the switching states presented in (4). The capacitor voltages are both the state and output vector to this model

$$\mathbf{x_c} = \mathbf{y_c} = [V_{c,a1}\ V_{c,a2}\ V_{c,a3}\ \cdots\ V_{c,c3}\ V_{c,c4}]^T \tag{6}$$

In the second model, the arm currents are considered as parameters within the prediction horizon, because a small change in the arm currents, as given by the first model, has a negligible effect on the capacitor voltages.

The discrete-time model of the system, using a sampling period of T_{s} = 25 μs is as follows:

$$\mathbf{x_i}(k + 1) = \mathbf{A_i}\mathbf{x_i}(k) + \mathbf{B_i}\mathbf{u}(k) \tag{7}$$

$$\mathbf{y_i}(k + 1) = \mathbf{C_i}\mathbf{x_i}(k + 1) \tag{8}$$

$$\mathbf{x_c}(k + 1) = \mathbf{A_c}\mathbf{x_c}(k) + \mathbf{B_c}\mathbf{u}(k) \tag{9}$$

$$\mathbf{y_c}(k + 1) = \mathbf{C_c}\mathbf{x_c}(k + 1) \tag{10}$$

The definition of the system matrices $\mathbf{A_i}$, $\mathbf{B_i}$, $\mathbf{C_i}$, $\mathbf{A_c}$, $\mathbf{B_c}$ and $\mathbf{C_c}$ can be found in Appendix A.

B. Control Algorithm

The switching scheme *switch and extrapolate* ("SE") is adopted, as described in [22], [26], with N_s of 1 to predict the states of the M2LC. In this scheme, an extrapolation of the predicted load current trajectories yields a prediction horizon, N_p, which is significantly longer than one without increasing the computational burden of the controller.

Given the current states, $\mathbf{x_i}(k)$ and $\mathbf{x_c}(k)$, load current bounds and previous switching state, $\mathbf{u}(k-1)$, the control scheme selects a switching state $\mathbf{u}(k)$ that will keep the load currents within bounds and minimize the variation in the capacitor voltages. The operation principle of the "SE" scheme is explained below:

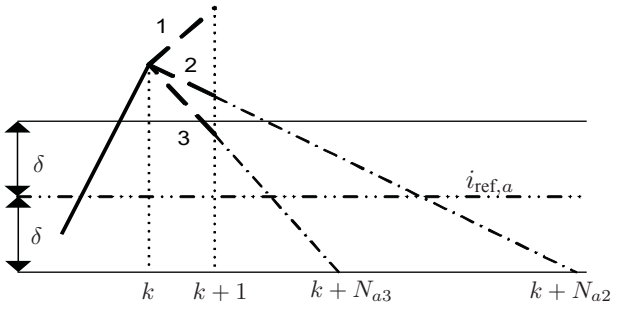
1) Given the last input $\mathbf{u}(k-1)$ and the current states, the arm currents and, as a result, the load currents are predicted at time-step $k+1$ using (7) and (8) for all switching sequences. This implements the first part, S, of the "SE" scheme. The load current ripple is determined for each phase by subtracting the predicted load current from the sinusoidal reference for all switching sequences, $i_{\text{rip},r}(k+1) = i_r(k+1) - i_{\text{ref},r}(k+1)$, $r \in \{a,b,c\}$, where $i_{\text{ref},r}(k+1)$ is the load current reference. As an example, for phases a and b, predicted trajectories of the load current for three switching sequences are shown in Fig. 2. Here, δ is one half of the allowable ripple band around the reference currents.
2) Determine candidate switching sequences with indices j, where $j \in \mathcal{J}$ and $\mathcal{J}$ is an index set, based on the predicted load currents and reject those switching sequences for which a load current violates bounds at $k+1$. Here, the candidate sequences are those switching sequences that yield current trajectories that are either inside of the bounds or their violation decreases with time. As an example, consider Fig. 2, in which the switching sequence 1 is not a candidate sequence because the load current violates the upper bound, for both phases a and b, at time-step $k+1$. On the other hand, the predicted load current at $k+1$ is predicted to be within the hysteresis bounds when selecting the third switching sequence, making it a candidate sequence. For the second sequence, the current at $k+1$ will remain outside of its bound for phase a, but its violation decreases from k to $k+1$, making it also a candidate sequence.
3) The candidate trajectories are then linearly extrapolated from time-step $k+1$ onwards until they violate the predefined band [27]. This implements the second part, E, of the "SE" scheme. This extrapolated length, N_j, is represented in multiples of T_s. Consider selecting sequence 2 at time-step k, the load current trajectories can be kept within the bounds for a length of $N_2 = \min(N_{a2}, N_{b2}, N_{c2})$, before requiring a new switching sequence at time-step $k+N_2$.
4) At the next stage, predict the capacitor voltages, using (9) and (10), for all the predetermined candidate sequences (item 2). These voltages are then extrapolated for the number of time steps determined in item 3. The capacitor voltages at time-step $k+N_j$, $j \in \mathcal{J}$ are denoted as terminal capacitor voltages, $V_{c,rn}(k+N_j)$.
5) The following cost function is evaluated for all the candidate sequences which are determined in step 2.

$$C_j = \lambda_1 \frac{||\mathbf{u}_j(k) - \mathbf{u}(k-1)||}{N_j} + \lambda_2 ||\mathbf{v}_{\text{cDiff}}(k+N_j)||_2^2 + \lambda_3 ||\mathbf{v}_{\text{cNom}}(k+N_j)||_2^2,\ j \in \mathcal{J} \tag{11}$$

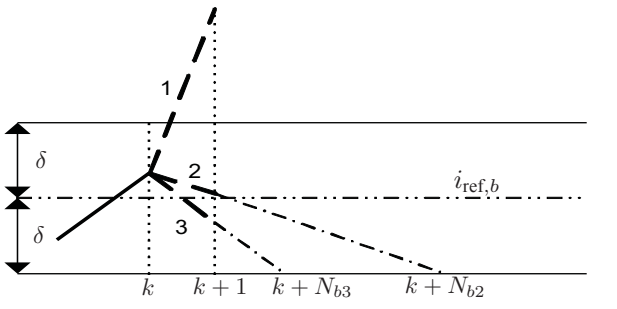
where,

$$\mathbf{v}_{\text{cDiff}}(k) = \begin{bmatrix} V_{c,a1}(k) - V_{c,a2}(k) \\ V_{c,a3}(k) - V_{c,a4}(k) \\ V_{c,b1}(k) - V_{c,b2}(k) \\ V_{c,b3}(k) - V_{c,b4}(k) \\ V_{c,c1}(k) - V_{c,c2}(k) \\ V_{c,c3}(k) - V_{c,c4}(k) \end{bmatrix} \quad \mathbf{v}_{\text{cNom}}(k) = \begin{bmatrix} V_{c,a1}(k) - \frac{V_\text{DC}}{2} \\ V_{c,a2}(k) - \frac{V_\text{DC}}{2} \\ V_{c,a3}(k) - \frac{V_\text{DC}}{2} \\ V_{c,a4}(k) - \frac{V_\text{DC}}{2} \\ V_{c,b1}(k) - \frac{V_\text{DC}}{2} \\ V_{c,b2}(k) - \frac{V_\text{DC}}{2} \\ V_{c,b3}(k) - \frac{V_\text{DC}}{2} \\ V_{c,b4}(k) - \frac{V_\text{DC}}{2} \\ V_{c,c1}(k) - \frac{V_\text{DC}}{2} \\ V_{c,c2}(k) - \frac{V_\text{DC}}{2} \\ V_{c,c3}(k) - \frac{V_\text{DC}}{2} \\ V_{c,c4}(k) - \frac{V_\text{DC}}{2} \end{bmatrix}$$

The first term in the cost function penalizes the number of switch transitions discounted over the prediction horizon, allowing one to minimize the number of switching transitions. It is evaluated by dividing the number of switch transitions by the length of the extrapolated trajectory. The second term in the cost function is used to minimize the difference in the capacitor voltages within the upper and lower arm, respectively. The third term minimizes the difference between the terminal capacitor voltages and one half of the supply voltage, $\frac{V_\text{DC}}{2}$. Omitting the second term may result in unsymmetrical



(a) Phase a



(b) Phase b

Fig. 2: Trajectories of the load currents (a) phase a and (b) phase b. Actual, predicted and extrapolated trajectories are shown as solid, dashed and dashed-dotted lines, respectively.

capacitor voltages within an arm, because the third term only sets a reference for the average value of the capacitor voltages.
Here, λ_1, λ_2 and λ_3 are the weighting coefficients and heuristic approach was followed to select their values.

6) The switching sequence with the minimum cost is selected and implemented at time-step k.

A receding horizon policy is implemented by repeating these steps at the next sampling instant. Furthermore, additional control objectives can be easily included by adding them to the cost function.

Total Demand Distortion (TDD) of the load current can be controlled by adjusting the ripple δ. There is a linear relationship between TDD and the δ band as presented in [22], where the TDD is a measure of the load current harmonic distortion.

IV. Performance Evaluation

Performance of the MPDCC scheme was investigated, using PLECS/SIMULINK, for a 2MVA three-level M2LC and compared with a vector control (VC) scheme with a pulse width modulator. In the latter scheme, load currents in abc frame were transformed into dq quantities, followed by comparison with their reference values of $i_{d,\text{ref}} = 1$ and $i_{q,\text{ref}} = 0$ and, finally, proportional-integral (PI) controllers were employed to generate voltage reference in each phase. The dq voltage references, were then transformed to abc domain and compared against carrier waveforms in phase disposition (PD) to generate the gating signals for the modules. The frequency of the carrier waveform was 750 Hz and a third harmonic was injected in the reference signals using a min-max approach that achieves the same switching sequences as space vector modulation [28]. The capacitor voltages were balanced by using a sorting algorithm, which was based on the polarity of the arm currents [4], [9], [17], [19]. For example, for a positive arm current the capacitor with lowest voltage was selected first, and conversely, the capacitor with the highest voltage was prioritized for a negative arm current. The circuit parameters used for the simulations are summarized in Table I, using $V_B = \sqrt{2/3}V_{ll}$ = 2449.49 V, $I_B = \sqrt{2}I_{rat}$= 544.47 A and f_B = 50 Hz as base quantities for the p.u. system.

A. Steady-State Performance

Fig. 3 shows the waveforms of the load currents with the MPDCC scheme, which shows that load currents are kept inside the bounds.

TABLE I: System parameters

Parameter		p.u.	SI
Output frequency	f_o	1	50 Hz
Supply voltage	V_{dc}	2.1229	5.2 kV
Grid Voltage	V_{ll}	1.2247	3 kV
Load current	i_r	0.7071	385 A
Capacitance	C_{rn}	11.3067	8 mF
Load resistance	R_l	0.0667	300 mΩ
Arm resistance	R	0.0222	100 mΩ
Load inductance	L_l	0.2	2.86 mH
Arm inductance	L	0.0698	1 mH

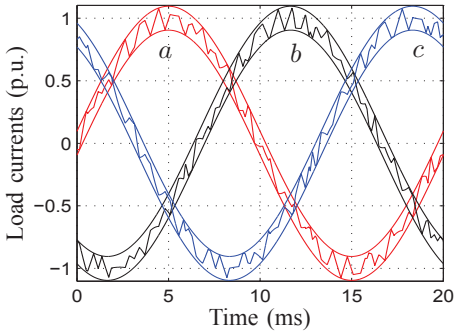
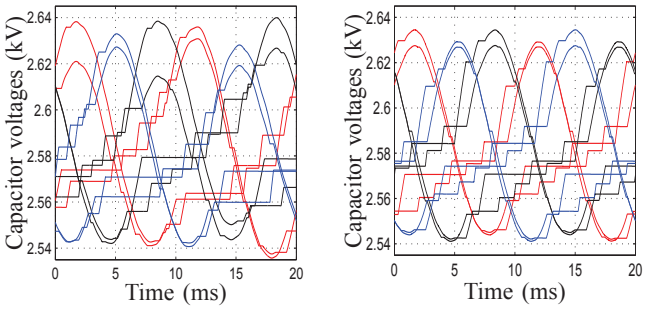


Fig. 3: Load currents with MPDCC for one sinusoidal period



(a) MPDCC (b) VC with PWM

Fig. 4: Capacitor voltages for one sinusoidal period

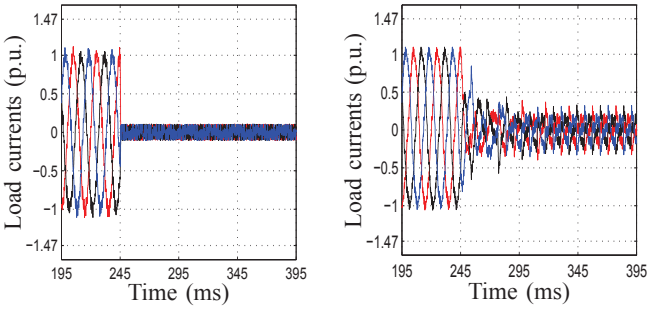
The capacitor voltages were balanced within 4% of their average value and Fig. 4 shows the voltage waveforms for one fundamental time period. In case of MPDCC, there are small fluctuations in the peaks of the capacitor voltages, however, the voltages are well balanced.

With the PWM scheme, the TDD of the load currents and the switching frequency are 7.86 % and 400 Hz, respectively. In constrast, MPDCC results in a sligtly lower TDD of 7.29 % and an average switching frequency of 385 Hz, where the latter is evaluated over a time period of 100 ms.

For the PWM scheme, the switching frequency cannot be reduced below a certain value, otherwise, with fixed switching instants, balancing of the capacitor voltages becomes an issue.

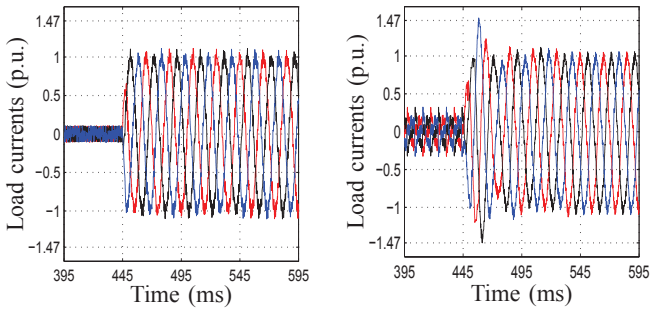
B. Performance during Transients

Initially, the converter was operating at rated load current before the reference of the load currents was changed to zero at time-instant $t = 245$ ms. At time-instant $t = 445$ ms,



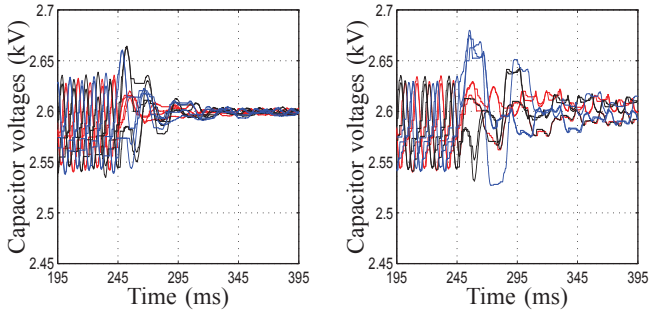
(a) MPDCC (b) VC with PWM

Fig. 5: Load currents during the power-down transient



(a) MPDCC (b) VC with PWM

Fig. 6: Load currents during the power-up transient



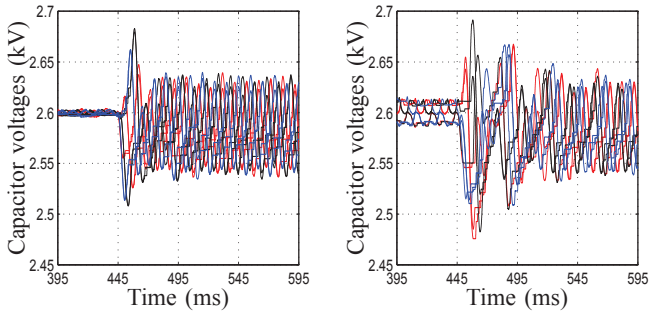
(a) MPDCC (b) VC with PWM

Fig. 7: Capacitor voltages during the power-down transient

the load current reference was changed back to 1 p.u. The load current ripple, $\delta = 0.1$ p.u., was not changed during the transient operation.

As shown in Fig. 5 and Fig. 6, MPDCC achieves a very fast current response both at power-down and power-up. It takes less than 3 ms to deliver the rated load currents. On the other hand, the PWM scheme provides a slow response. Fig. 6 shows that the load currents overshoot at power-up before settling at their nominal values. With PWM scheme, the current response might not be further improved because increasing PI gains beyond certain values will result in an unstable oscillations in the load currents.

With the MPDCC scheme, the capacitor voltages, as shown in Fig. 7 and Fig. 8, are well balanced both at power-down and power-up. After power-up, the capacitor voltages settle within 4% of the average voltage value in less than three sinusoidal periods. Whereas, with the PWM scheme,



(a) MPDCC (b) VC with PWM

Fig. 8: Capacitor voltages during the during the power-up transient

the capacitor voltages exhibit large oscillations both at power-down and power-up.

During the transients, the converter rapidly changes the arm currents to meet the load current requirements. During this period, the arm inductors and capacitors exchange energy, resulting in an overshoot of the capacitor voltages at power-down and power-up. This overshoot in the voltage can be further minimized by controlling the rate of change of the load current's reference trajectory or with an appropriate design of the arm inductor.

V. Conclusions

MPDCC with a long prediction horizon for the control of the M2LC has been presented in this paper. It has been shown that the MPDCC requires a single control loop, without a modulator, to control the load currents within tight bounds around their sinusoidal references, balance the capacitor voltages and minimize the switching frequency in comparison to existing hierarchical control schemes. Simulated results have been presented to validate the viability of the proposed control technique. Furthermore, it has been shown that the MPDCC scheme achieves very fast current responses during transients, such as power-up and power-down. The capacitor voltages have been kept close to their reference values both during transients and steady-state operating conditions. In addition, comparison with a vector control PWM scheme has shown that improvements in performance with the MPDCC.

Appendix A
The Discrete-Time Matrices of the Models

$$\mathbf{A_i} = e^{\mathbf{T}^{-1}\mathbf{F_i}T_s} \tag{12}$$

$$\mathbf{B_i} = \mathbf{F_i}^{-1}\mathbf{T}(\mathbf{A_i} - \mathbf{I}_1)\mathbf{T}^{-1}\mathbf{G_i} \tag{13}$$

$$\mathbf{T} = \begin{bmatrix} L & L & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & L & L & 0 & 0 & 0 \\ -L & -L & -L & -L & 2L & 0 & 0 \\ -L_l & L+L_l & L_l & -L-L_l & 0 & 0 & 0 \\ 2L_l & -2L-2L_l & L_l & -L-L_l & L & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{F_i} = \begin{bmatrix} -R & -R & 0 & 0 & \frac{2R}{3} & 0 & 0 \\ 0 & 0 & -R & -R & \frac{2R}{3} & 0 & 0 \\ R & R & R & R & \frac{-4R}{3} & 0 & 0 \\ R_l & -R-R_l & -R_l & R+R_l & 0 & \frac{3}{2} & \frac{-\sqrt{3}}{2} \\ -2R_l & 2R+2R_l & -R_l & R+R_l & -R & \frac{-3}{2} & \frac{-\sqrt{3}}{2} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega \\ 0 & 0 & 0 & 0 & 0 & \omega & 0 \end{bmatrix}$$

Here, $\mathbf{I}_1$ represents an identity matrix of a relevant order.

$$\mathbf{A_c} = e^{\mathbf{F_c}T_s} \tag{14}$$

$$\mathbf{B_c} = \mathbf{F_c}^{-1}(\mathbf{A_c} - \mathbf{I}_2)\mathbf{G_c} \tag{15}$$

$$\mathbf{G_i} = \begin{bmatrix} -\frac{2}{3}V_{c,a1} & -\frac{2}{3}V_{c,a2} & -\frac{2}{3}V_{c,a3} & -\frac{2}{3}V_{c,a4} & \frac{V_{c,b1}}{3} & \frac{V_{c,b2}}{3} & \frac{V_{c,b3}}{3} & \frac{V_{c,b4}}{3} & \frac{V_{c,c1}}{3} & \frac{V_{c,c2}}{3} & \frac{V_{c,c3}}{3} & \frac{V_{c,c4}}{3} \\ \frac{V_{c,a1}}{3} & \frac{V_{c,a2}}{3} & \frac{V_{c,a3}}{3} & \frac{V_{c,a4}}{3} & -\frac{2}{3}V_{c,b1} & -\frac{2}{3}V_{c,b2} & -\frac{2}{3}V_{c,b3} & -\frac{2}{3}V_{c,b4} & \frac{V_{c,c1}}{3} & \frac{V_{c,c2}}{3} & \frac{V_{c,c3}}{3} & \frac{V_{c,c4}}{3} \\ \frac{V_{c,a1}}{3} & \frac{V_{c,a2}}{3} & \frac{V_{c,a3}}{3} & \frac{V_{c,a4}}{3} & \frac{V_{c,b1}}{3} & \frac{V_{c,b2}}{3} & \frac{V_{c,b3}}{3} & \frac{V_{c,b4}}{3} & -\frac{2}{3}V_{c,c1} & -\frac{2}{3}V_{c,c2} & -\frac{2}{3}V_{c,c3} & -\frac{2}{3}V_{c,c4} \\ 0 & 0 & -V_{c,a3} & -V_{c,a4} & 0 & 0 & V_{c,b3} & V_{c,b4} & 0 & 0 & 0 & 0 \\ 0 & 0 & V_{c,a3} & V_{c,a4} & 0 & 0 & 0 & 0 & 0 & 0 & -V_{c,c3} & -V_{c,c4} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\mathbf{F_c} = -\frac{1}{C_{rn}R_{\text{cap}}}\mathbf{I}_2 \tag{16}$$

$$\mathbf{C_c} = \mathbf{I}_2 \tag{17}$$

$$\mathbf{C_i} = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ -1 & 1 & -1 & 1 & 0 \end{bmatrix} \tag{18}$$

$$\mathbf{G_c} = \frac{1}{C_{rn}}\text{diag}(i_{\text{aP}},\ i_{\text{aP}},\ i_{\text{aN}},\ i_{\text{aN}},\ i_{\text{bP}},\ i_{\text{bP}},\ i_{\text{bN}},\ i_{\text{bN}},\ i_{\text{cP}},\ i_{\text{cP}},\ i_{\text{cN}},\ i_{\text{cN}}) \tag{19}$$

Here, $\mathbf{I}_2$ represents an identity matrix of a relevant order and diag(...) is a square diagonal matrix with entries inside the brackets at its main diagonal [$\diagdown$].

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