Comparison of Hybrid Control Techniques for Buck and Boost DC-DC Converters

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***Abstract*—Five recent techniques from hybrid and optimal control are evaluated on two power electronics benchmark problems. The benchmarks involve a number of practically interesting operating scenarios for fixed-frequency synchronous DC-DC converters. The specifications are defined such that good performance can only be obtained if the switched and non-linear nature of the problem is accounted for during the design phase. A non-linear action is featured in all methods either intrinsically or as external logic. The designs are evaluated and compared on the same experimental platform. Experiments show that the proposed methods display high performances, while respecting circuit constraints, thus protecting the semi-conductor devices. Moreover, the complexity of the controllers is compatible with the high-frequency requirements of the considered application.**

***Index Terms*—DC-DC, Hybrid control, Model Predictive Control, Sampled Data Control, Robust Control.**

I. Introduction

This paper presents an investigation of hybrid techniques for the synthesis of high performance controllers for the fixed-frequency buck (step-down) and boost (step-up) DC-DC converters. The proposed circuits present a number of challenges, starting with the switched nature of the system dynamics, which directly accounts for their hybrid characteristics. Even if the classic averaging approach [1] were to be applied, the resulting model of the boost converter would still be non-linear, and the non-minimum phase behaviour and input/state constraints additionally complicate the controller design process. In classical approaches, the non-minimum phase behaviour of the boost converter and the maximum admissible current constraint of both buck and boost converters have been successfully dealt with by reducing the feedback gain or by employing cascaded voltage and current control [2]. The former solution reduces the controller dynamic performance, while both voltage and current transducers are necessary for the indirect control approach. The recent past has seen the emergence of digital control [3]–[10] as an increasingly viable option for power electronics. The corresponding availability of computational power has created interest in the investigation of alternative and innovative control methods that could overcome the limitations of classical approaches.

In the context of the current work five different design methods have been derived and evaluated on the same experimental platforms under a variety of operating conditions by considering response times and disturbance rejection capabilities. In particular, three of the five design methods are applied to both the buck and boost topologies, while one method is applied only to the buck and one only to the boost topology. The benchmark examples investigated in this paper were first defined in [11], [12] whereto the interested reader is referred for a comprehensive survey of related works in the power electronics area.

The various control methodologies that are summarized in Tab. I are presented by five research groups, identified according to their affiliations (CRAN, ETH, KTH, LTH, SUPELEC). CRAN considers a new approach for model predictive control (MPC) where a one-step Newton algorithm is used to track a reference trajectory. The reference trajectory is updated by an adaptive loop. ETH utilizes (hybrid) piecewise affine (PWA) approximations of the converter dynamics within an explicit model predictive control framework inclusive of duty cycle and inductor current constraints. The KTH team uses an extension of sampled data $\mathcal{H}_\infty$-control theory to pulse width modulated systems. An outer feedback loop takes care of state and control constraints and averaged sampling is used in order to achieve robust tracking. LTH employs the relaxed dynamic programming formulation from [13], where it is possible to take state and control constraints into account. The approximate optimal controller provides guaranteed robustness and stability margins. SUPELEC employs a stabilizing approach using a Lyapunov function deduced from energetic considerations to obtain the Boolean value of the control variable. Four approaches are of discrete-time nature (CRAN, ETH, KTH, LTH), where the converter switches are controlled through the duty cycle of a pulse width modulator (PWM),

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while the SUPELEC approach is of continuous-time nature, where the switches are directly controlled through a binary variable.

method denomination	group	type	buck	boost
Adaptive-predictive control approach	CRAN	DPWM	IV-A	-
Explicit model predictive control	ETH	DPWM	IV-B3	IV-B4
Sampled data control for robust tracking	KTH	DPWM	IV-C3	IV-C4
Relaxed dynamic programming	LTH	DPWM	IV-D	IV-D
Stabilizing control approach	Supelec	CD	-	IV-E

TABLE I
SUMMARY OF ASSOCIATIONS BETWEEN GROUPS, METHODS AND BENCHMARK PROBLEMS; DPWM INDICATES DISCRETE-TIME APPROACHES BASED ON PWM, CD CONTINUOUS-TIME APPROACHES BASED ON DIRECT SWITCH CONTROL.

The paper is organized as follows: Section II presents the buck and boost converters, whereas Section III formally defines the associated control problem. The approaches proposed by the different groups are detailed in Section IV. Implementation issues are addressed in Section V. Experimental results are displayed in Section VI and finally conclusions are drawn in Section VII.

II. CONVERTER DESCRIPTION

A. Topologies

The system schematics are shown in Fig. 1. The converters are supplied by an unregulated DC voltage source and they provide a regulated DC voltage to a variable ohmic load. The converters comprise each an inductor L, a capacitor C and a switching cell. The synchronous buck converter under investigation is composed by two MOSFET switches T_L and T_H which are operated synchronously. The boost converter is composed by the MOSFET T_L and the diode D_H. The coil value and the minimum load current are such that the coil current does not reach zero in normal operation and the converter always operates in continuous conduction. The switching cells therefore only present two modes of operation for both cases.

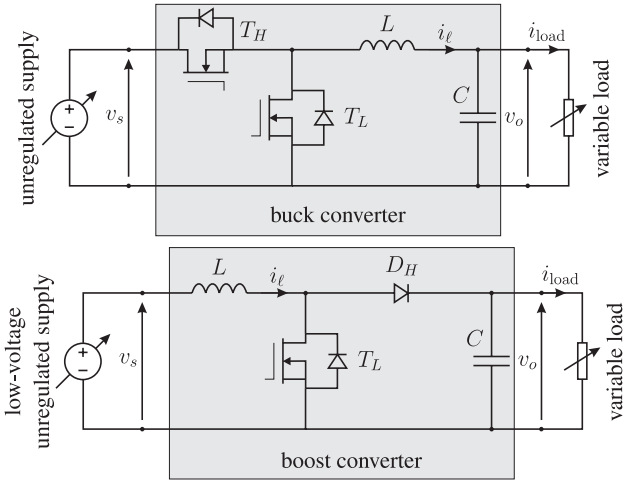


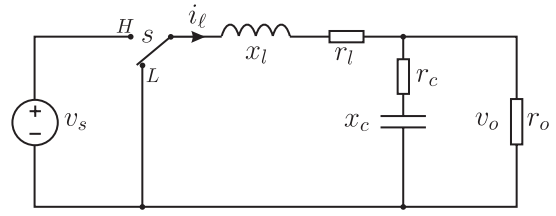
Fig. 1. Converter system

B. Physical system phenomena

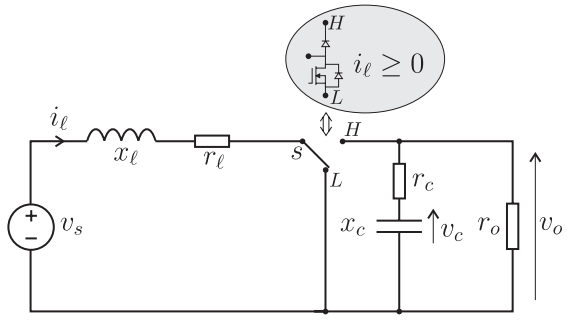
The converter behaviour during the switching is complex and a model reproducing precisely the system behaviour would comprise several stray inductors associated to the connecting tracks and cables and also the parasitic capacitors mainly associated to the semiconductor devices. The coil is highly non-linear and displays hysteretic behaviour due to the magnetic cycle of its core. In normal operation, these phenomena are however mostly negligible at the control level and therefore not taken into account in the following.

C. Lumped parameter model

The coil non-linearities are neglected as in normal operation the control scheme must prevent entering the saturation region. The switches are also considered as ideal. At each switching instant, the stray inductors and parasitic capacitors cause an oscillation that typically cannot be captured by the control scheme or that simply appears as noise. These phenomena are therefore also neglected. The circuit models that are obtained after these simplifications are the lumped parameter switched models represented in Fig. 2: x_ℓ represents the linear inductance value associated to the coil L, whose losses are accounted for by r_ℓ, and x_c and r_c respectively represent the capacitance and equivalent series resistor (ESR) of C. The circuits are thus lumped in that the losses have been concentrated in the parasitic values r_ℓ and r_c. Additionally, r_o denotes the output load resistor. The switching stages of the



(a) buck converter model



(b) boost converter model

Fig. 2. Lumped parameter circuit used for control synthesis

converters are formalized through the switch s representing the dually operated semiconductor components. By defining $x(t) = [i_\ell(t)\ v_c(t)]^T$ as the state vector, where $i_\ell(t)$ is the inductor current and $v_c(t)$ the capacitor voltage, and with a given duty cycle $d[k]$ for the k-th period, the systems are described by the following pair of affine continuous-time state-

space equations:

$$\dot{x}(t) = \begin{cases} F_1 x(t) + f_1 v_s(t), & s = 1 \\ F_2 x(t) + f_2 v_s(t), & s = 0. \end{cases} \quad (1)$$

where the first equation holds when s is in the H position (respectively L) for the buck (respectively boost) and the second when it is in the L position (respectively H) for the buck (respectively boost). The matrices F_1, F_2, f_1 and f_2 are given for the buck by

$$F_1 = F_2 = \begin{bmatrix} -\frac{1}{x_\ell}(r_\ell + \frac{r_o r_c}{r_o + r_c}) & -\frac{1}{x_\ell}\frac{r_o}{r_o + r_c} \\ \frac{1}{x_c}\frac{r_o}{r_o + r_c} & -\frac{1}{x_c}\frac{1}{r_o + r_c} \end{bmatrix} \quad (2)$$

$$f_1 = \begin{bmatrix} \frac{1}{x_\ell} \\ 0 \end{bmatrix}, f_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad (3)$$

and for the boost by:

$$F_1 = \begin{bmatrix} -\frac{r_\ell}{x_\ell} & 0 \\ 0 & -\frac{1}{x_c(r_o + r_c)} \end{bmatrix} \quad (4a)$$

$$F_2 = \begin{bmatrix} -\frac{1}{x_\ell}(r_\ell + \frac{r_o r_c}{r_o + r_c}) & -\frac{1}{x_\ell}\frac{r_o}{r_o + r_c} \\ \frac{1}{x_c}\frac{r_o}{r_o + r_c} & -\frac{1}{x_c}\frac{1}{r_o + r_c} \end{bmatrix} \quad (4b)$$

$$f_1 = f_2 = \begin{bmatrix} \frac{1}{x_\ell} \\ 0 \end{bmatrix}. \quad (5)$$

The output voltage $v_o(t)$ across the load r_o is expressed as a function of the states through

$$\begin{cases} v_o(t) = g_1^T x(t), & s = 1 \\ v_o(t) = g_2^T x(t), & s = 0. \end{cases} \quad (6)$$

where

$$g_1 = g_2 = \frac{r_o}{r_o + r_c} \begin{bmatrix} r_c & 1 \end{bmatrix}^T \quad (7)$$

for the buck and

$$g_1 = \begin{bmatrix} 0 & \frac{r_o}{r_o + r_c} \end{bmatrix}^T \quad (8a)$$

$$g_2 = \begin{bmatrix} \frac{r_o r_c}{r_o + r_c} & \frac{r_o}{r_o + r_c} \end{bmatrix}^T \quad (8b)$$

for the boost.

D. Modulation scheme

The converter switch control signal must be driven by a pulse sequence in order to maintain the output voltage average value. PWM is employed for most control schemes (CRAN, ETH, KTH, LTH). In that case, the converter operation is characterized by the constant *switching frequency* f_p, (*switching period* T_p) of the PWM, which is equal to the controller sampling frequency f_s (*sampling period* T_s). The DC component of the output voltage is then regulated through the duty cycle $d[k]$, which is defined by $d[k] = \frac{t_{\text{on}}[k]}{T_p}$, where $t_{\text{on}}[k]$ represents the interval within the k-th switching period during which s is in the H position for the buck converter, respectively L for the boost.

The approach presented by SUPELEC directly controls the switches through a boolean variable, thus the sampling frequency f_s and the switching frequency f_p are in general not equal.

III. CONTROL PROBLEM

The main control objective is to steer the DC component of the output voltage to its reference value $v_{o,\text{ref}}$. The output voltage must be maintained in the face of measurable voltage source variations and immeasurable load changes. This objective is subject to hard constraints that must be enforced by the control:

1) a limit $i_{\ell,max}$ is imposed on the inductor current as a safety measure to avoid saturation and semiconductor damages,
2) when the control input is a PWM duty cycle $d[k]$, it must satisfy the physical constraint $d[k] \in [0, 1]$[1].

There are also other constraints, which restrain the controller structure:

1) The switching frequency has an upper bound in order to respect the converter maximum rating (such as thermal limitations) and a lower bound to respect the output voltage ripple bound ($\pm 1\%$ in our case):
   - for the approaches relying on PWM this constraint is inherently enforced,
   - for the other approaches the switching criterion must enforce this frequency constraint.
2) the quantities that can be measured and used for control feedback are the source and output voltages and the current of the inductor,
3) the design must be robust to variations in the voltage source and load and to parametric uncertainty,
4) the controller must be simple to implement and should not require excessive computation times.

The five design methods presented in the next section will be derived and assessed on the basis of the above specifications in Sections VI.

IV. CONTROL METHODS

Analysis and design of DC-DC converters are normally done using small signal approximations of averaged models [1]. The averaging technique is convenient to use but it offers only a low frequency approximation of the true dynamics where the discontinuous effect introduced by the switching is ignored. A number of alternative modeling techniques summarized in Tab. I will be discussed in this section including several types of PWA models and a sampled data model.

A. An adaptive-predictive control approach (CRAN)

MPC offers attractive solutions for the regulation of such hybrid systems. This control methodology has reached a certain maturity which is witnessed by its successful implementation in industry and by the development of a theoretical foundation in many books and articles, see, for example, [14], [15], [16] and the references therein. We consider the MPC scheme presented in Fig. 3, where the control law is implemented using PWM as discussed in II-D and where all other blocks will be described below.

[1]In practice the interval is even smaller in some case to maintain proper gate driver operation and avoid narrow pulses

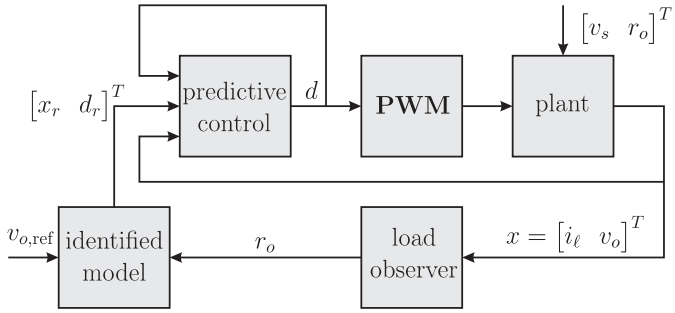


Fig. 3. CRAN predictive control scheme overview.

The method presented in this subsection is applied to the buck converter, thus as mentioned in section II-C $F_1 = F_2$, $f_2 = 0_{2\times 1}$, $g_1 = g_2$ and we will only use F_1 and g_1 to simplify notations. The approach can however be extended to the boost case using an average model obtained from the convex hull of all vector fields, i.e. $F_{\text{av}}(x,d) = d(F_1\, x(t) + f_1\, v_s) + (1-d)(F_2\, x(t) + f_2\, v_s), \quad d \in [0,1]$. The operating points of the converter are then determined as the equilibrium points of F_{av} [17].

1) Generation of the reference trajectories: Starting from initial state, the goal being to track the output reference $v_{o,\text{ref}}[k]$, the first objective is to generate a feasible reference trajectory x_r from the identified system (1), which will be used as the reference to track in the predictive control part. This indirect approach is motivated by the fact that it is easier to tune the controller to track a feasible precomputed response (i.e. to filter reference trajectories that are not feasible, such as steps, in order to improve the system response) than to respond to an *infeasible* step.

Assuming that the state of the buck converter is periodic at steady state, its average value over a switching-period can be considered constant [18]. The duty cycle in the steady-state d_r^∞ can therefore be computed from the average model

$$\begin{aligned} \dot{\overline{x}}_r(t) &= F_1 \overline{x}_r(t) + f_1 v_s d_r \\ \overline{v}_o(t) &= g_1^T \overline{x}_r(t) \end{aligned} \tag{9}$$

At steady state, $\dot{\overline{x}}_r(t) = 0$ and for a given average reference $\overline{v}_o(t) = v_{o,\text{ref}}$, the duty cycle d_r^∞ is deduced from (9) by

$$d_r^\infty = -\frac{v_{o,\text{ref}}}{g_1^T F_1^{-1} f_1 v_s} \tag{10}$$

The corresponding state value at the beginning of the period is computed from (1):

$$x_r^\infty = \left(I - e^{F_1 T_s}\right)^{-1} F_1^{-1} e^{F_1 T_s} \left(I - e^{-F_1 T_s d_r^\infty}\right) f_1 v_s \tag{11}$$

From d_r^∞ and x_r^∞, a reference trajectory x_r can be defined.

Using the notation $x_r[k] = x_r(kT_s)$ and $d_r[k] = d_r(kT_s)$, the state x_r at the instant $k+1$ can be computed as

$$x_r[k+1] = e^{F_1 T_s} x_r[k] + F_1^{-1} e^{F_1 T_s} \left(I - e^{-F_1 T_s d_r[k]}\right) f_1 v_s \tag{12}$$

In order to obtain the duty cycle $d_r[k]$, a one step receding horizon procedure is used. Thus, we minimize the following quadratic error

$$J_r = \|x_r[k] - x_r^\infty\|^2_{Q_r} + \mu_r (\Delta d_r[k])^2 \tag{13}$$

with respect to the duty cycle variations $\Delta d_r[k] = d_r[k] - d_r[k-1]$. Here $\|x\|^2_{Q_r} := x^T Q_r x$ is a quadratic norm, Q_r is a positive-definite matrix and μ_r is a positive constant.

The optimization problem (13) can be solved either analytically from the necessary condition

$$\frac{\partial J_r}{\partial \Delta d_r} = 0 \tag{14}$$

or using a Newton algorithm.

The constraint $i_\ell[k+1] \leq i_{\ell,\max}$ is checked a-posteriori. When $i_\ell[k+1] < i_{\ell,max}$ is not satisfied, a new duty cycle must be computed as

$$d_r[k] = \text{argmin}(\|i_\ell[k+1] - i_{\ell,\max}\|). \tag{15}$$

The optimal duty cycle $d_r[k]$ is the result of the optimization shown before. $d_r[k]$ is only used to compute the trajectory $x_r[k+1]$. This state will be used as a reference for the predictive control.

2) Predictive control: Once the reference trajectory $x_r[k+1]$ is available, a classical tracking problem should be solved.

We consider a prediction - correction structure as the control strategy for the buck converter. The control is determined by minimizing a quadratic function of the prediction error between the reference trajectory $x_r[k+1]$ and a predicted state $x_p[k+1]$. A correction using past measurements is used to reduce the sensitivity to the noise and the unmodeled parameters. The function to be minimized is

$$J_p = \| \left(x_p[k+1] - x_r[k+1]\right) \|^2_{Q_p} + \mu_p (\Delta d)^2 \tag{16}$$

and the minimization is done with respect to the duty cycle variations $\Delta d = d[k] - d[k-1]$. In the definition of J_p, μ_p is a positive constant and Q_p is a positive definite matrix. The predicted state x_p is obtained at $k+1$ from $x_p[k]$ as

$$x_p[k+1] = \Phi(x_p[k], d[k]) + \Lambda(x_p[k], x[k]) \tag{17}$$

where $x[k]$ is the measurement from the real system, Φ indicates the future states without correction

$$\Phi(x_p[k], d[k]) = e^{F_1 T_s} x_p[k] + F_1^{-1} e^{F_1 T_s} \left(I - e^{-F_1 T_s d[k]}\right) f_1 v_s \tag{18}$$

and Λ is a correction term of the form

$$\Lambda(x_p[k], x[k]) = L g_1^T (x[k] - x_p[k]) \tag{19}$$

where $L \in \mathbb{R}^{1\times n}$ is the observer gain. Although the system switches, its dynamics does not change ($F_1 = F_2$), which implies that L can be easily computed using a pole placement.

The minimization of J_p can be done analytically from $\partial J_p / \partial \Delta d = 0$ or numerically using the Newton algorithm with only one iteration. This control is applied to the identified system and the real system in order to obtain $x[k]$, and $x_p[k]$ for the next period.

3) Load observer: Load estimation should be done in order to ensure robustness of the control law. Besides, in the predictive control, the values of the identified parameters should be near the values of the real parameters in order to obtain an accurate prediction.

The identification process can be written as a least-squares optimization problem of a quadratic function

$$\min_{r_0} \quad \varepsilon(x, x_p) = \min_{r_0} \quad (x - x_p)^T Q (x - x_p). \tag{20}$$

We can use a simple gradient algorithm to obtain the value of the load.

B. Explicit model predictive control (ETH)

1) Explicit Model Predictive Control: The major advantage of MPC is its straight-forward design procedure. Given a discrete-time control model of the system, including constraints, one only needs to set up an objective function that incorporates the control objectives [19]. The control action at each time step is then obtained by measuring the current state and minimizing the objective function over a finite prediction horizon subject to the equations and constraints of the model. The first value stemming from the predicted optimal sequence of control inputs is then applied to the system and the procedure is repeated at the successive sampling instant. Depending on the model and on the length of the prediction horizon used in the objective function, this minimization problem varies considerably in complexity. For piecewise affine (PWA) linearly constrained systems with cost functions based on one or infinity norms, this optimal value is PWA and it can *equivalently* be obtained through an explicit solution approach, through which the optimization problem is pre-solved off-line for every possible instance, rendering a look-up table which is searched on-line to directly yield the desired optimal input [20]. This bears the advantage of avoiding the need to perform any on-line optimization, thus making the MPC paradigm applicable also for systems with shorter sampling times or with limited computational power.

2) Constrained Finite Time Optimal Control for DC-DC Converters: The proposed MPC scheme implies the formulation of a constrained finite-time optimal control (CFTOC) problem to be solved with a receding horizon policy. Assuming that a discrete-time control model of the DC-DC converter is available (see Sections IV-B3 and IV-B4 respectively for the buck and boost topologies), in the following the derivation of a cost function capturing the required objectives is presented and the explicit solution procedure of the resulting optimization problem is briefly presented.

The control objectives are to regulate the output voltage to its reference as fast and with as little overshoot as possible, or equivalently, to minimize the absolute *scaled* output voltage error $v'_{o,\mathrm{err}}[k] = |v'_o[k] - v'_{o,\mathrm{ref}}|$, where $v'_o[k] = \frac{v_o[k]}{v_s}$ and $v'_{o,\mathrm{ref}} = \frac{v_{o,\mathrm{ref}}}{v_s}$: the scaling of the values over v_s will be made clear in Sections IV-B3 and IV-B4. Let $\Delta d[k] = |d[k] - d[k-1]|$ indicate the absolute value of the difference between two consecutive duty cycles. This term is introduced in order to reduce the presence of unwanted chattering in the input when the system has almost reached stationary conditions by penalizing any additional variations in the duty cycle. Define the penalty matrix $Q = \mathrm{diag}(q_1, q_2)$ with $q_1, q_2 \in \mathbb{R}^+$ and the vector $\varepsilon[k] = [v'_{o,err}[k], \Delta d[k]]^T$. Consider the objective function

$$J(D[k], x'[k], d[k-1]) = \sum_{l=0}^{N-1} \|Q\ \varepsilon[k+l|k]\|_1 \tag{21}$$

penalizing the predicted evolution of $\varepsilon[k+l|k]$ from k over the horizon N using the 1-norm. The control input at time-instant k is then obtained by minimizing the objective function (21) over the sequence of duty cycles $D[k] = [d[k], \ldots, d[k+N-1]]^T$ subject to the model equations and constraints featured in Sections IV-B3 and IV-B4 and the current limitation $i'_\ell[k] \leq i'_{\ell,max}$, where $i'_{\ell,max} = \frac{i_{\ell,max}}{v_s}$; the resulting problem is referred to as the CFTOC problem.

Multi-parametric programming is employed to solve this optimization problem off-line for a range of parameters. In [21] it is shown how to reformulate and solve a discrete-time CFTOC problem as a multi-parametric program featuring the state vector as a parameter, yielding an explicit state-feedback controller. Note that the CFTOC problem is not only a function of $x'[k]$, but also of the last control move $d[k-1]$; furthermore, as it is necessary to solve the CFTOC problem for all possible values of $v'_{o,\mathrm{ref}}$ and $i'_{\ell,max}$, the scaled output voltage reference and inductor current maximum limit also enter the augmented state vector, which therefore is 5-dimensional. As proven in [21] the optimal state-feedback control law $d^*[k]$ is a piecewise affine function of the (augmented) state vector defined on a polyhedral partition of the feasible (augmented) state space, commonly referred to as a look-up table. As mentioned in Section IV-B1, such a look-up table facilitates implementation, since computing the control input amounts to determining the polyhedron in which the measured state lies and then simply evaluating the corresponding affine control law. Additionally, the derived feedback controller allows deriving an explicit representation of the closed-loop system, for which a Lyapunov function certifying exponential stability can be sought *a posteriori* through the method presented in [22].

In order to avoid introducing additional complexity into the CFTOC problem posed above, load variations are dealt with by using the state-feedback controller (derived for a time-invariant and nominal load), to which a loop comprising a Kalman filter that features a correcting integral action [23], [24] is added. For this, the reformulated (nominal) continuous-time model is augmented by a third state that tracks the output voltage error, and the Kalman filter is used to estimate it. In a last step, the output voltage reference $v'_{o,\mathrm{ref}}$ is adjusted by the tracked voltage error. The overall control structure is shown in Fig. 4

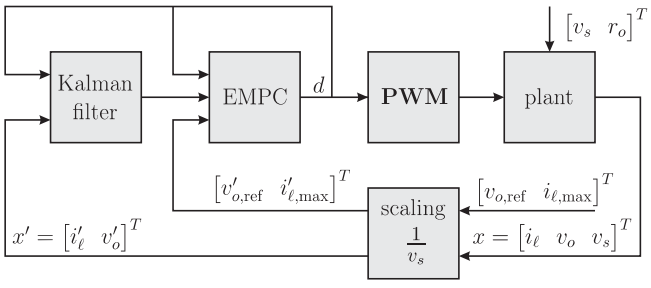


Fig. 4. ETH explicit model predictive control scheme overview.

3) Control Model Derivation for the Buck Converter: Polyhedral Piece Wise Affine (PWA) systems are defined by partitioning the state-space into polyhedra and associating with each polyhedron an affine state-update and output function [25]. In previous publications [8], [26]–[28] the notion of the ν-resolution model was introduced as an effective way to describe the switched hybrid dynamics of the buck converter. This modeling approach leads to a discrete-time PWA converter model that is valid for the whole operating regime of the system and provides a direct trade-off between the accuracy of the obtained model and its related complexity through the choice of the resolution ν. As shown in [24], the converter PWA model uses a transformed converter state vector $x' = [i'_\ell, v'_o] = [\frac{i_\ell}{v_s}, \frac{v_o}{v_s}]$ comprising the inductor current and the *output* voltage, both scaled over the voltage source: since v_s appears as a linear term in the system equations, it is effectively removed from there so that it does not show up in the control model and therefore does not have to be included as a separate parameter in the explicit state-feedback controller.

For $\nu = 3$, the discrete-time PWA state-update map of the ν-resolution model amounts to

$$x'[k+1] = \Phi^3 x'[k] + \begin{cases} \Phi^2\Psi 3 d[k], & d[k] \in [0, \frac{1}{3}] \\ \Phi^2\Psi + \Phi\Psi 3(d[k] - \frac{1}{3}), & d[k] \in [\frac{1}{3}, \frac{2}{3}] \\ \Phi^2\Psi + \Phi\Psi + \Psi 3(d[k] - \frac{2}{3}), & d[k] \in [\frac{2}{3}, 1] \end{cases} \quad (22)$$

$$0 \le d[k] \le 1 \quad (23)$$

with $\Phi = e^{F\tau_s}$, $\Psi = \int_0^{\tau_s} e^{F(\tau_s - t)} dt\, f$ and $\tau_s = \frac{T_s}{3}$. Since (22) refers to the transformed state vector, the matrix and vector F and f are different from the ones in (1) and (2); see [24] for exact expressions. The discrete-time control model of the buck converter employed in Section IV-B2 for the derivation of the associated CFTOC problem is thus represented by (22) and (23).

4) Control Model Derivation for the Boost converter: From an implementation point of view, it is preferable if all the states used in the prediction model are directly measurable. Thus, the capacitor voltage is replaced by the output voltage in the state vector which leads to setting $x(t) = [i_\ell(t)\ v_o(t)]^T$ by correspondingly reformulating (1). Additionally, to obviate the requirement of accounting explicitly for voltage source variations, v_s is removed from the model equations by redefining the scaled state vector $x'(t) = [i'_\ell(t)\ v'_o(t)] = [\frac{i_\ell(t)}{v_s}\ \ \frac{v_o(t)}{v_s}]$, similarly as in Section IV-B3.

Next, a discrete-time model is formulated by employing a sampling interval equal to the switching period T_s. The employed method considers a direct least squares fitting (LSF) approximation over several regions of the control input of the exact system update equations, yielding a PWA description of the associated non-linear expressions. These can be written as

$$x'[k+1] = \Theta(d[k])x'[k] + \Gamma(d[k]) \quad (24)$$

where $\Theta(d[k])$ and $\Gamma(d[k])$ are matrices that depend nonlinearly on the duty cycle $d[k]$, calculated by integrating the converter equations from $t = k$ to $t = k + 1$.

Expression (24) is approximated by determining the matrices $\bar{A}_m$, $\bar{B}_m$ and $\bar{f}_m$ that describe the system in terms of

$$x'[k+1] = \bar{A}_m x'[k] + \bar{B}_m d[k] + \bar{f}_m \quad (25a)$$

$$\text{if } d[k] \in D_m \quad m = 1, \ldots, M \quad (25b)$$

$$0 \le d[k] \le 1 \quad (25c)$$

and that minimize the sum of quadratic error terms

$$\|\Theta(d[k])x'[k] + \Gamma(d[k]) - (\bar{A}_m x'[k] + \bar{B}_m d[k] + \bar{f}_m)\|^2 \quad (26)$$

over a gridded series of points $x'[k]$ in the state space $[0, i'_{\ell,\lim}] \times [0, v'_{o,\lim}]$, where D_m are the M intervals $[0, \frac{1}{M}], ..., [\frac{M-1}{M}, 1]$, and $i'_{\ell,\lim}$, $v'_{o,\lim}$ are the limit values of the scaled inductor current and output voltage over the considered range. The discrete-time control model of the boost converter employed in Section IV-B2 for the derivation of the associated CFTOC problem is thus represented by (25a), (25b) and (25c).

It should be highlighted that because of the non-minimum phase behaviour of the boost converter a considerably longer horizon length N is chosen than for the buck to capture the inverse step response and account for it within the optimization horizon. As this would increase the complexity of the problem considerably, a simple move-blocking scheme is used whereby $d[k] = d[k+1] = \ldots = d[k+N-1]^T$ throughout the horizon.

C. Sampled Data Control for Robust Tracking (KTH)

Discrete time models of DC-DC converters have an advantage over conventional averaged models since they take the switched nature of the plant into account and therefore have potential for better performance. However, the discrete time model has a drawback since it only describes the state at the switching instants. Since the inter sampling behaviour is not accounted for, control design based on the discrete time model may lead to subharmonic oscillations, where the period of the (periodic) steady state solution is larger than the switch period (see [29] for an example in the model class considered in the current paper).

1) The sampled data model: The fact that a subharmonic solution may appear suggests that the discrete-time model is insufficient. We therefore consider design based on a sampled data (SD) model. The SD model gives a precise description of the state at the switching instants, but also includes a lifted signal which describes the inter sampling behaviour. Thus, the SD model allows the effect of continuous time disturbances and model uncertainty to be represented exactly in an equivalent discrete-time model.

Within the SD framework we consider $\mathcal{H}_\infty$ synthesis and we therefore include an external disturbance w in the system dynamics. The disturbance is chosen as an independent current source at the output to model uncertainty in the load.

The SD model is of the form

$$\begin{aligned} x[k+1] &= \Phi(d[k])x[k] + \Gamma_1(d[k]) + \Gamma_2(d[k])\hat{w}[k] \\ \hat{y}[k](\theta) &= (\Psi(d[k])x[k])(\theta) + \Delta_1(d[k])(\theta) + (\Delta_2(d[k])\hat{w}[k])(\theta) \\ \psi[k] &= \begin{bmatrix} \psi_1[k] \\ \psi_2[k] \end{bmatrix} \end{aligned} \quad (27)$$

where $x[k] := x(kT_s)$ is the system state, $\hat{y}[k](\theta)$ and $\hat{w}[k](\theta)$ are lifted versions of the performance output y and the disturbance signal w (see Fig. 5). Several operators that appear in the lifting representation are mappings between function spaces. We have

$$\begin{aligned} &\Phi(d) : \mathbb{R}^n \to \mathbb{R}^n, && \Psi(d) : \mathbb{R}^n \to L_2[0, T_s) \\ &\Gamma_1(d) : \mathbb{R} \to \mathbb{R}^n, && \Delta_1(d) : \mathbb{R} \to L_2[0, T_s) \\ &\Gamma_2(d) : \mathbb{R} \to L_2[0, T_s), && \Delta_2(d) : L_2[0, T_s) \to L_2[0, T_s) \end{aligned}$$

where the dependence on d is nonlinear.

The signal $\psi[k]$ is the input to the controller available at time kT_s. The control input consists of two parts. $\psi_2[k] := x(kT_s)$ is obtained by sampling the state and $\psi_1[k] := S_{\rm av}(v_o)[k]$ is obtained by sampling the output voltage using a so-called average sampler which is defined as

$$S_{\rm av}(f)[k] := \frac{1}{T_s} \int_{(k-1)T_s}^{kT_s} f(\tau) \mathrm{d}\tau$$

The average sampler is introduced to ensure that the output voltage tracks the voltage reference $v_{o,\rm ref}$. Without the average sampler it is not possible to make the tracking robust against parameter variations, see [30] for a discussion.

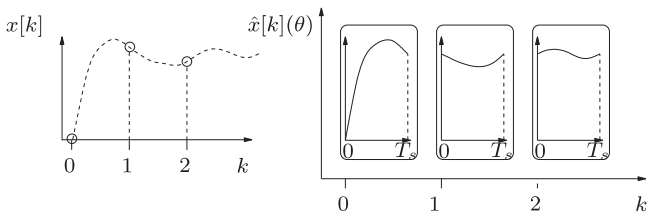


Fig. 5. Sampled signal $x[k]$ (left) and lifted signal $\hat{x}[k](\theta)$ (right).

At steady state when the duty cycle is constant, the state of a DC-DC converter will attain a periodic solution such that the average of the voltage equals $v_{o,\rm ref}$. The control objective is to ensure asymptotic convergence to this nominal T_s-periodic solution (and corresponding stationary duty cycle) (x^0, d^0) which satisfies the tracking condition

$$\lim_{k\to\infty} S_{\rm av}(v_o)[k] = \frac{1}{T_s} \int_0^{T_s} v_o^0(\tau) \mathrm{d}\tau = v_{o,\rm ref} \qquad (28)$$

where v_o^0 is the periodic output voltage corresponding to x^0. We want to satisfy (28) robustly against e.g., parameter uncertainties and the disturbance w. This motivates us to introduce the integrator state

$$e_d[k] := \sum_{i=0}^{k-1} (\psi_1[i] - v_{o,\rm ref})$$

and consider the objective of satisfying

$$\int_0^t \|y(\tau) - y^0(\tau)\|^2 \mathrm{d}\tau + \sum q \|e_d[k]\|^2 \le \gamma^2 \int_0^t \|w(\tau)\|^2 \mathrm{d}\tau \qquad (29)$$

for all $t \ge 0$ and for all solutions to the converter dynamics. The chosen performance output y defines the cost function and is used to tune the controller.

The $\mathcal{H}_\infty$ criterion (29) can be equivalently stated as a discrete-time $\mathcal{H}_\infty$ optimization problem by using the lifted system representation (27). However, the problem is highly nonlinear and in general intractable for optimization. In the sequel we therefore consider a linearization of (27) together with a linear quadratic approximation of (29). This results in a new type of sampled data $\mathcal{H}_\infty$ control problem which was solved in [31], [32]. Depending on the measurements available, the solution yields either a state feedback vector or a dynamic output feedback controller.

2) State and input constraints: The sampled data controller is surrounded by an outer loop which, if necessary, will adjust the duty cycle and system state. The outer loop is motivated by a number of reasons. Firstly, the SD controller has integral action and we therefore add an anti-windup structure. If the linear feedback saturates, then the term

$$\Delta = d^0 + K(x[k] - x^0) - d[k]$$

is used to modify the integrator state in a linear fashion;

$$e_d[k+1] = e_d[k] + (\psi_1[k] - v_{o,\rm ref}) + c\Delta$$

where $c > 0$. Secondly, the state constraint $i_\ell \le i_{\ell,max}$ is not considered in the SD synthesis and needs to be dealt with by some additional control structure. We add a one-time step MPC algorithm which (if necessary) adjusts the duty cycle and which can be implemented as a nonlinearity, see [12] for details. Finally, the SD controller is designed for a fixed nominal input voltage. Changes in the input voltage are handled by the integrator state, but the response is made faster by using measurements of the input voltage in a feed forward fashion. We note that the outer loop remains inactive under normal operation.

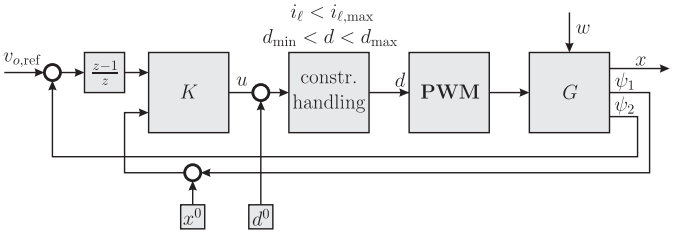


Fig. 6. Sampled data feedback control configuration.

3) Application to the buck converter: For the buck converter we assume we have access to the full state and consider the (approximate) sampled data $\mathcal{H}_\infty$ problem discussed above. The solution yields a linear feedback vector K which is implemented with the integrator as illustrated in Fig. 6. We note that if the full state were not available, the $\mathcal{H}_\infty$ problem formulation would yield a dynamic output feedback controller.

4) Application to the boost converter: The output voltage of the boost converter is non-minimum phase with respect to the duty cycle. This problem and the problem of multiple steady-state equilibriums can be bypassed by formulating a current (rather than voltage) regulation problem. However, in the current regulation approach one must choose an inductor current reference that necessarily depends on the load which must be estimated.

Our goal is to achieve robustness to uncertainty and disturbances in the load and we also want to be able to deal with more complex loads than purely resistive. We therefore prefer voltage regulation. The non-minimum phase behaviour of the boost can be made less pronounced by including both the inductor current and the output voltage in the output signal y which enters in the performance index (29).

D. Relaxed Dynamic Programming (LTH)

Except for special cases, the computations required to solve a synthesis problem by means of *exact* dynamic programming are prohibitive. The only possibility is to resort to approximations. The approximation algorithms that we present in this section were developed in [33], where the reader can find more details. More information on Relaxed Dynamic Programming techniques can also be found in [34], [35]. The choice of algorithms was made for several reasons. First, an important design criterion for the problem considered in this paper is constraints on system variables. This can be accounted for in the method we use. Moreover, the controller we design will approximate a *stationary* optimal controller. As such, it will inherit robustness margins from the optimal controller.

Since the algorithms in [33] require that the system dynamics is affine, we need to approximate the converter dynamics (1) with such systems. The modeling technique presented below, which may be referred to as a robust affine approximation, is proposed in order to take into account, already at the modeling stage, the switched nature of the converter and the fact that the converter is parameterized by unknown parameters.

1) Robust Affine Model Approximation: The exact state propagation between time $k\,T_s$ and $(k+1)\,T_s$ is given by

$$x[k+1] = \Phi(d[k], r_o)x[k] + \Gamma(d[k], r_o) \tag{30}$$

which can easily be found by integrating the switched dynamics over one period. The load parameter r_o has been appended to emphasize that the matrices depend on the load. We need to approximate this nonlinear system with an affine system

$$x[k+1] = \hat{\Phi}x[k] + \hat{\Gamma}d[k] + \hat{\nu} \tag{31}$$

When the model (30) is approximated with the model (31), the largest pointwise error can be expressed as

$$J = \sup ||\hat{\Phi}x + \hat{\Gamma}d + \hat{\nu} - (\Phi(d, r_o)x + \Gamma(d, r_o))|| \tag{32}$$

where the supremum is taken over $(x, d, r_o) \in \mathbb{X} \times \mathbb{D} \times \mathbb{L}$, where $\mathbb{D} = [0 \quad 1]$ and $\mathbb{X} = [0 \quad i_{\ell,lim}] \times [0 \quad v_{o,lim}]$ is the set of states on which the model should be approximated. $\mathbb{L}$ is the set of values that the load can assume. Naturally, we would like to minimize J. The robust approximation problem is to compute

$$\min J(\hat{\Phi}, \hat{\Gamma}, \hat{\nu}) \tag{33}$$

over $(\hat{\Phi}, \hat{\Gamma}, \hat{\nu})$. Our ability to solve this problem depends on the choice of norm and the description of the set $\mathbb{X} \times \mathbb{D} \times \mathbb{L}$. The candidates are those that correspond to a finite dimensional convex optimization problem. For the purpose of this paper we shall consider a simple choice. Define a finite grid of points $G \subset \mathbb{X} \times \mathbb{D} \times \mathbb{L}$, for each $g = [x_g^T \quad d_g \quad r_g] \in G$ define

$$b(g) = \Phi(u_g, r_g)x_g + \Gamma(d_g, r_g), \text{ and } A(g) = g \otimes I \tag{34}$$

where $\otimes$ denotes the Kronecker product of two matrices. If we also define $y = \text{vec}([\hat{\Phi} \quad \hat{\Gamma} \quad \hat{\nu}])$, i.e. the decision variables are stacked in the vector y, the approximation problem becomes

$$\min_y \max_{g \in G} ||A(g)y - b(g)|| \tag{35}$$

which is the same as

$$\begin{aligned} &\min_{y,t} \quad t \\ &||A(g)y - b(g)|| \leq t, \quad \forall g \in G. \end{aligned}$$

If the norm is either $||\cdot||_\infty$ or $||\cdot||_1$ this is an LP. If the norm is $||\cdot||_2$ the problem is a second order cone problem. In any case, it is an easily solvable finite dimensional convex optimization problem. See [36] for a discussion on convex optimization.

2) Control Design: To simplify notation we define $e(x) = \begin{bmatrix} x^T & 1 \end{bmatrix}^T$. Our goal is to synthesize a feedback controller

$$d[k] = \mu(x[k])$$

such that the total cost $V = \sum_{k=0}^{\infty} l(x[k], d[k])$ is approximately minimized, under an additional constraint on the inductor current, $x_1[k] \leq i_{\ell,\max}$ and also $0 \leq d[k] \leq 1$. The following stage cost was used

$$l(x, d) = q_1|v_o - v_{o,\text{ref}}| + q_2|d[k] - d[k-1]|$$

where q_1 and q_2 are positive weights. The penalty on consecutive control values was introduced to force the duty cycle to become constant when v_o has reached the output reference. Thus, an extra state $x_e[k] = d[k-1]$ was introduced. We used relaxed value iteration to solve for a stationary approximate value function $\hat{V}$ satisfying

$$\beta V^* \leq \hat{V} \leq \alpha V^*$$

where $\beta \leq 1 \leq \alpha$ are constants and V^* is the optimal total cost function. The parameters α and β can, just as the step-cost function parameters, be regarded as control design parameters. As β decreases or α increases the controller complexity decreases. Thus the choice of these parameters is a compromise between complexity and performance.

The approximate value function is given by a max of linear functions $\hat{V} = \max_{p \in P} p^T e(x)$ where P is a set of vectors. The corresponding explicit piecewise affine feedback controller is given by $\mu(x) = L_p(x)^T e(x)$, where $p(x) = \text{argmax}_{p \in P} p^T e(x)$. To compute the controller value $\mu(x)$ at a state x we need to take the following steps

1) Find $p \in P$ such that $p^T e(x)$ is maximal
2) Set $\mu(x) = L_p^T e(x)$

Thus, we have to do a linear search over the table P. Consequently, it is important to keep the table P as small as possible, and for this purpose a reduction algorithm has been outlined in [33].

Finally, the errors introduced by the model approximation were handled by an outer integrator loop that adjusts the voltage reference. The integrator was activated only when the voltage v_o was sufficiently close to its reference.

The complete closed loop system is depicted in Fig. 7.

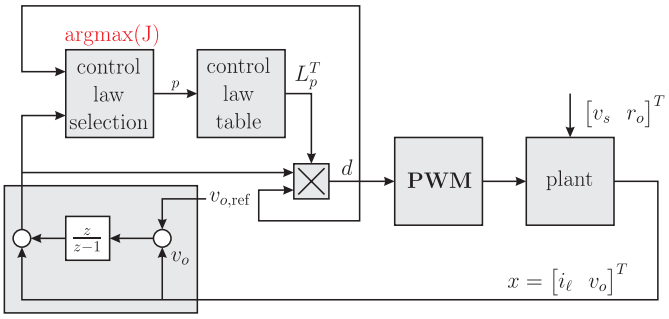


Fig. 7. LTH control structure overview: an explicit control law is found from a look-up table.

E. Stabilizing Control Approach (SUPELEC)

Unlike the previously presented methods, the stabilizing control, which is a continuous time approach directly computes the Boolean control variable (without PWM), using a common Lyapunov function candidate, such that the system is asymptotically stable. A Port Control Hamiltonian (PCH) formulation which accounts for the system energy is used. For switching systems, the PCH formulation is written as follows:

$$\dot{x} = [J(\rho) - R(\rho)]\frac{\partial H(x)}{\partial x} + G(\rho)u \tag{36}$$

where $x \in \mathbb{R}^n$ is the state vector containing the energy variables (fluxes in the inductors and charges in the capacitors). $\rho \in \{0,1\}^p$ is the Boolean control variable. The matrix J is skew-symmetric, (i.e., $J = -J^T$) it describes the power interconnections of the model, R is nonnegative and corresponds to the dissipating part of the system, G is the power input matrix and u represents the power sources present in the system. H represents the energy stored in the system. This is also called the Hamiltonian of the system. If the constitutive relations of the storage elements are linear, which is most often the case in power converters, they can be represented by the matrix Q_c and the Hamiltonian of the system is such that:

$$\frac{\partial H\,(x)}{\partial x} = Q_c\, x = z \tag{37}$$

The matrix Q_c satisfies $Q_c = Q_c^T > 0$ and in the simple cases, it is also diagonal. The vector $z = Q_c x$ represents the co-state variables (currents in the inductors and voltages on the capacitors).

In the case of power converters, the state equation is affine with respect to the Boolean variables [37]. Thus, the matrices $J(\rho)$, $R(\rho)$ and $G(\rho)$ can be written as

$$\begin{aligned} J\,(\rho) &= J_0 + \sum_1^p \rho_i J_i, R\,(\rho) = R_0 + \sum_1^p \rho_i R_i \\ G\,(\rho) &= G_0 + \sum_1^p \rho_i G_i \end{aligned} \tag{38}$$

where ρ_i are the components of the control vector ρ and p is its dimension.

The approaches in the literature which are based on Lyapunov functions consider, in general, linear systems with a common equilibrium point [38], [39]. In the case of power converters, each configuration may or may not have a different equilibrium point and physical considerations enable establishing a common Lyapunov function. This function depends on the control objective, which has to be defined first. It is obtained using the same approach as with an average model. Thus the control variable is no more boolean but continuous and bounded ($0 \leq \rho_{0i} \leq 1$). The control objective corresponds to an admissible reference for the system which is defined by solving (36) for $\dot{x} = 0$. It is a value for the co-state variable $z_0 = Q_c x_0$ which must satisfy the constraint

$$0 = (J\,(\rho_0) - R\,(\rho_0))\, z_0 + G\,(\rho_0)\, E \tag{39}$$

if there is a $\rho_0 \in \mathbb{R}^p, 0 \leq \rho_{0i} \leq 1$. According to the properties of this equation and the respective dimension or x and ρ, for one ρ_0, the equilibrium point can be unique or not, and for ρ_0 any point of the state space can be an equilibrium point or not [40].

For a function V to be a Lyapunov function for a system in a point x_0 it must be positive anywhere except in x_0 and its derivative must always be negative. If such a control law is applied, then x will converge asymptotically toward x_0. The candidate Lyapunov function has the form

$$V\,(x, x_0) = \tfrac{1}{2}\,(x - x_0)^T\, Q_c\,(x - x_0)\,. \tag{40}$$

Because the matrix Q_c is unique for all the modes of the system, V is positive and continuous for every x and it is nil only in x_0. Its derivative depends on the control variable and using (36) and (38) it can be expressed as

$$\dot{V}_\rho = -\,(z - z_0)^T\, R\,(\rho)\,(z - z_0) + \sum_{i=1}^{p} w_i, \tag{41a}$$

$$w_i = (z - z_0)^T\,((J_i - R_i)\, z_0 + g_i u)\,(\rho_i - \rho_{0i}). \tag{41b}$$

Due to the fact that $R(\rho)$ is a non-negative matrix, the first term is always negative. Because $0 \leq \rho_{0i} \leq 1$ the sum can be made negative by choosing an appropriate value for each Boolean ρ_i such that each product w_i is negative. Multiple state feedback control strategies can be envisaged for attaining this goal [40]. In the following a maximum descent strategy is used as it yields better results in terms of computation time due to a simpler expression of the commutation surfaces. It consists in choosing, at each time, the value of ρ such that all the terms in the sum are negative or zero. Commutation surfaces are then p hyperplanes defined by

$$T_i = (z - z_0)^T((J_i - R_i)z_0 + g_i u) = 0. \tag{42}$$

In the case of the boost converter, as there is only one control variable, the sum from expression (41) has only one term T, which, according to (42) becomes

$$T = \frac{r_o i_{\ell,0}}{r_c + r_o}\,(v_o - v_{o,0}) - \frac{r_o r_c i_{\ell,0} + r_o v_{o,0}}{r_c + r_o}\,(i_\ell - i_{\ell,0}) \tag{43}$$

where the admissible reference is computed by solving (39) for the nominal value of the output voltage $v_{o,0}$.

Because this strategy requires an infinite bandwidth a dead-zone is created with the help of a parameter ϵ. This way the derivative of the Lyapunov function may take positive values

for a limited amount of time. The new commutation surfaces are thus defined by $T = \epsilon$. The period and the amplitude of the oscillations around the reference depend on this parameter.

To ensure the robustness with regard to the parameter variations and to improve the start-up performance, the admissible reference is modified on-line. A new value for the current reference, i_{0n}, is computed under the form

$$i_{0n} = i_{\ell,0} + (v_{o,0} - v_o)\frac{k}{r_o} \tag{44}$$

where k is a parameter. i_{0n} is bounded between 0 and the maximal admissible value for the current in the inductor. The discrete-time implementation of the control scheme is depicted in Fig. 8.

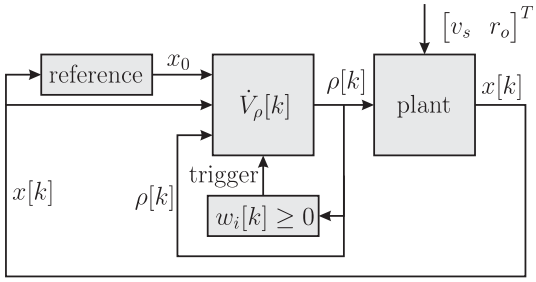


Fig. 8. Discrete-time implementation of SUPELEC control scheme. Control input is evaluated when block $w_i \geq 0$ triggers the control law. Reference block adjust reference trajectory for robustness to disturbance and improved transient performance.

V. Implementation

A. Power converters

A buck and a boost converter have been realized in order to evaluate the different control methods. Each converter is composed of a MOSFET power module that provides a converter leg with a low parasitic inductor. A filtering capacitor placed at the converter supply input reduces the supply voltage fluctuations. Additionally, a small fast capacitor is placed right next to the power module terminals in order to have a good switching cell with a low parasitic inductor.

B. Gate drivers

The gate drivers are used to amplify the control signals in order to apply the appropriate voltage and current to the MOSFET gates. The driver of the transistor T_H — the transistor connected to the supply's positive terminal — uses a boost trap circuit to draw power from the auxiliary supply. As the boost trap capacitor is charged when the low transistor is on, the duty cycle has to be limited to 95% in order to ensure a sufficient energy transfer. At the duty cycle lower bound, it is not desirable to have duty cycles smaller than approximately 1% as they only produce narrow pulses and converter losses. As the two transistors are complementary an interlock time is necessary to avoid short circuit of the leg during the transition between the two switches. This is ensured by the appropriate logic at the cost of a small distortion in the voltage pattern.

C. Controller hardware and software setup

Two DSP control boards were made available for the implementation:

1) a 32 bit 225MHz floating point DSP from Texas Instrument TMS320C6713,
2) a 16 bit 600MHz fixed point DSP from Analog Device Blackfin.

The floating point platform is most convenient since it allows for easy translation of algorithms in C into floating point arithmetics. This limits the programming effort and reduces the risk of numerical saturation and overflow. This platform is often used in academia because of the above reasons. The fixed point platform requires more development effort in order to avoid saturations and overflows. However it provides more computation power — which was the reason to have this second platform — and the code can directly be used on a simple industrial controller that does not support floating point arithmetic.

On both platforms, the same C code template has been used. This template initializes the DSP and all its devices and sets up an interrupt at the sampling frequency which acquires the data from the AD converters, runs the control algorithm and applies the calculated duty cycle to the converter. To ensure a more consistent implementation of the various methods, the task related to the controller synthesis thus only pertains to the part between the acquisition of the digitalized measurement and the application of the duty cycle.

D. Delay issues

The sampling frequency is equal to the switching frequency, 20 kHz. A four channel AD converter is used to acquire and convert the output voltage, supply voltage and coil current. The duration of the analog-to-digital converter sampling and conversion process is 5 μs. As the 50 μs sampling time is short considering the computation power available for this kind of applications, the duration of all control steps is crucial and represented in Fig. 9. There are four important instants which are: τ_0, the beginning of the PWM voltage pattern; τ_1 the sampling instant; τ_2 the instant when the sampled measurement is available and when consequently the control algorithm can start; the new input is available in τ_3 but is only updated in τ_0. This last aspect needs some clarification. The PWM logic would become more complex if the input is permitted to safely change during the period and this would lead to a variable sampling and to phenomena which are difficult to tackle. This means that we must ensure that the new input is available before τ_0 (i.e. $\tau_3 < \tau_0$) in order to avoid introducing an additional delay in the control.

The sampling instant τ_1 and the beginning of the voltage pattern τ_0 are very often simultaneous, which introduces a delay of exactly one period in the control. This leaves less than one sampling period for the control algorithm to compute the next duty ratio. This common practice was selected for all methods in order to show that they can be implemented using a controller of limited computation power.

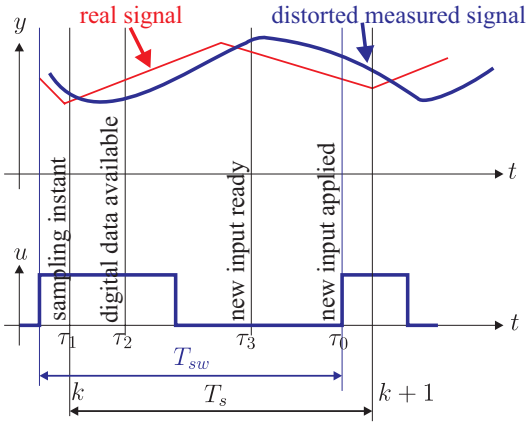


Fig. 9. Time diagram of the control process events.

E. Implementation complexity and computation time

1) Qualitative complexity analysis: From the point of view of the implementation, the form and complexity of the different control laws vary:

1) (CRAN) The control law was obtained analytically and features matrix exponentials. As the matrix exponentials cannot practically be used for the targeted application, they are approximated using a 2^{nd} degree Taylor series. The approximated control law then amounts to compute a few matrix and vector multiplications. The implementation of the load estimation uses a basic gradient descent algorithm.
2) (ETH) The control law amounts to evaluating $N_{st}+1$ affine functions that are 5-dimensional, N_{st} being the depth of the search tree (5-12 in this case).
3) (KTH) The main part of the control law consists of a 2-dimensional state feedback. An outer loop performs a simple test and if necessary adjusts the control to maintain the limit on the peak current.
4) (LTH) The control law amounts to evaluating N_r+1 affine functions that are 4-dimensional, N_r being the number of linear functions used to represent the approximate cost function.
5) (SUPELEC) The control law amounts to evaluating a second order polynomial in the state variables and control input. As described in section IV-E, the reference is adjusted on-line in order to increase the dynamic performance and ensure robustness to load variations.

In addition to these specific aspects ETH, KTH, and LTH use an external integrator loop.

2) Quantitative comparison: Three methods have been implemented using the 32-bit floating point DSP (CRAN, ETH, KTH, SUPELEC) as it was more convenient. As LTH systematically evaluate all regions, more computation power was required and it has been implemented on the 16-bit fixed point DSP. Finally one of the four former methods (ETH) has been ported on the fixed point DSP in order to check that the results are equivalent on both platforms. Tab. II summarizes the computation times defined as $\tau_3-\tau_2$. These times reflects the observation of the qualitative analysis performed in V-E1.

	$\tau_3-\tau_2$		f_s	f_p
Group	*floating point platform* μs	*fixed point platform* μs	kHz	kHz
CRAN	14.6-16.6	-	20	20
ETH	12.7-15.2	1.8-2.8	20	20
KTH	7.6-7.8	-	20	20
LTH	($\approx$ 200)	15.4	20	20
SUPELEC	2.7	-	120	≈ 8

TABLE II
CONTROL ALGORITHM COMPUTATION TIME.

VI. EXPERIMENTAL RESULTS

A. Definition of the benchmarks tests

The design methods presented in Section IV have been validated on an experimental platform with the following nominal parameter values $x_c = 100\mu$F, $x_l = 2$mH, $r_c = 0.1\Omega$ and $r_l = 0.5\Omega$. For PWM based methods, the switching frequency is $f_s = 1/T_s = 20$kHz. The nominal source voltage is $v_s = 25$V for the buck and $v_s = 50$V for the boost. The control objective is to keep the output voltage at the reference level, $v_{o,\text{ref}} = 25$V for the buck, $v_{o,\text{ref}} = 50$V for the boost, and to make sure that the inductor current does not exceed the limit $i_{\ell,\max} = 2.5$A. The nominal load is $r_o = 50\Omega$ for the buck and $r_o = 200\Omega$ for the boost.

A few relevant performance indices were selected for the benchmark:

1) start-up transient; this is a good indicator of the general performance of the controller,
2) load transient; the load is subject to large variations during operation and therefore the load transient is a good indicator for DC-DC converters,
3) line transient; the supply voltage is subject to large variations during operation,
4) robustness to parameters which are not well known and affect the dynamics (capacitor, inductor),
5) computation time.

Some measurements were grouped to limit the number of presented plots:

1) Start-up and load transients are shown on the same plot for 3 different reference voltages in Fig. 10 and 14, side by side for the different groups;
2) A robustness evaluation is shown in Fig. 11 and 15, where three different filter capacitors are used during the start-up transient;
3) Start-up and line transients are shown in Fig. 12 and 16.

B. Methods' specific parameters for the buck topology

1) CRAN: The parameters for the method are

$$Q_r = \begin{bmatrix} 1 & 0 \\ 0 & 2000 \end{bmatrix} \quad Q_p = \begin{bmatrix} 1 & 0 \\ 0 & 500 \end{bmatrix} \qquad (45)$$
$$\mu_r = 5.0 \qquad \mu_p = 0.5$$

where the $(2,2)-$ blocks of the matrices Q_r and Q_p are chosen relatively large to ensure tracking of the output voltage reference.

2) ETH: The model (22) with $\nu = 3$ was employed for the controller synthesis. For the cost function, the penalty matrix was chosen to be $Q = diag(10, 1)$ and the prediction horizon $N = 4$. As explained in Section IV-B the explicit state-feedback controller is defined in a 5-dimensional space, with a polyhedral partition featuring 105 regions.

3) KTH: To ensure robust tracking of the output voltage reference, the signal y in the $\mathcal{H}_\infty$ cost criterion (29) was chosen as $y = v_o$ and the weights were chosen as $q = 0.17$ and $\gamma = 2.2$. The corresponding linear quadratic approximate problem was solved and a feedback vector K was obtained. As explained in Section IV-C, the feedback was implemented with an anti wind-up structure where the gain was $c = 0.45$.

4) LTH: The weights in the step-cost function were chosen as $q_1/q_2 = 1/3$. An approximate cost function $\hat{V}^{23}$ was found after 23 value function iterations, with relaxation parameters $\beta = 0.6$ and $\alpha = 2.8$. After reduction, the size of the resulting look-up table was 102.

C. Methods' specific parameters for the boost topology

1) ETH: The model (25) was derived with $M = 3$ PWA dynamics, with the intervals D_i being $[0, 0.45]$, $[0.45, 0.6]$ and $[0.6, 0.95]$. For the cost function, the penalty matrix was chosen to be $Q = diag(10, 1)$ and the prediction horizon $N = 18$. As explained in Section IV-B the explicit state-feedback controller is defined in a 5-dimensional space, with a polyhedral partition featuring 122 regions.

2) KTH: The non minimum phase characteristics of the boost converter imply that the current should be included in the cost criterion. Thus, the signal y in (29) was chosen as $y = [0.5\ 1]x$. The weights were chosen to be $q = 2$, $\gamma = 3$ and the anti wind-up gain was chosen as $c = 0.5$.

3) LTH: The weights were $q_1/q_2 = 1/5$ and an approximate cost function $\hat{V}^{38}$ was found after 38 value function iterations with relaxation parameters $\beta = 0.4$ and $\alpha = 3.2$. After reduction, the size of the look-up table was 130.

4) SUPELEC: A discrete-time version of the control law featured by equation (43) was implemented with the maximum achievable sampling rate, 120 kHz. The period and the amplitude of the oscillations around the reference depend on the parameter ϵ, which was tuned to the value $\epsilon = 5$ in order to respect the maximum admissible switching frequency and the maximum capacitor voltage ripple.

D. Experimental results evaluation for the buck topology

All control methods globally fulfill the objective. They quickly reach the desired reference while respecting the current limitation. We will here analyze the experimental results and remark on some similarities and distinctions.

The methods display a different degree of conservativeness regarding the current constraint. The current is more or less kept at its limit during the transient and the variation is mainly depending on the method aggressiveness (flatter → most varying: LTH - ETH - KTH - CRAN). Some violation of the current constraint can be observed for CRAN.

The start-up swiftness varies according to the way the current constraint is applied (faster → slower: KTH - ETH/LTH - CRAN). A little overshoot can however be observed during the start-up in the methods by ETH/KTH. This is caused by the outer integral loop.

It can be observed as a general trend that the voltage deviation during the load transient is small and increases with the output voltage, see Fig. 10. The maximum voltage deviation during the load transient is: CRAN $\pm 0.4V$, ETH $+0.5V - 0.4V$, LTH $\pm 0.5V$, KTH $+0.7V - 0.5V$. CRAN uses a load observer and therefore reaches steady state faster after a load transient.

All methods are robust to a large capacitor variation, see Fig. 11. No significant deviation from the nominal behavior is observed. As for the nominal start-up transient a more pronounced overshoot due to the gain of the outer integral loop is observed for ETH/KTH.

The voltage deviation during the line transient mainly depends on how the supply voltage is accounted for in the control, see Fig. 12. The maximum voltage deviation during the load transient is: ETH $\pm 0.2V$, LTH $+0.2V - 0.55V$, KTH $+0.45V - 0.55V$, CRAN $+0.45V - 0.9V$. ETH scales the state over the input voltage, which makes the controller less sensitive to the supply transient.

Some simulation results have been selected in Fig. 13. The simulations feature the same operating conditions as the experiments and have been performed in Matlab$^{\mathrm{TM}}$ using the model in Section II-C with the above nominal values and with delay due to measurement, conversion, and computation included in the model. The simulations show close agreement with the experiments and only small differences can be observed when some very fast phenomena occur.

It has to be noted that even if the different controllers are based on different approaches, their performances are very similar. An analysis of the results show that most differences are not critically related to the selected approach. Some factors that affect the results can be identified as follow:

1) Controller structure: a part of the control characteristics is related to the control structure, such as the use or absence of observer in the loop or how the supply voltage is accounted for. The observer was necessary to obtain good results with the CRAN approach and the input voltage scaling reduced the sensitivity to input voltage changes in the ETH method. However, both the observer and the scaling idea are not specifically linked to one approach and could be used together with all methods with minor modifications, thus leading to different results.

2) Controller tuning: a different tuning could have lead to another classification of the methods independently of the structure of the control. It is moreover difficult to obtain a controller that has good ratings for all performance indices.

3) Outer integral loop tuning: there is unavoidable uncertainty linked to the model structure and the parameter values. Several methods use an additional integral loop to compensate for this uncertainty and this loop is mainly responsible for the observed overshoot and the slow compensation of static errors.

4) Noise sensitivity: the results are significantly affected by the trade-off between aggressiveness and sensitivity. This is particularly critical for power electronics applications since the level of noise is relatively high. The noise is even more

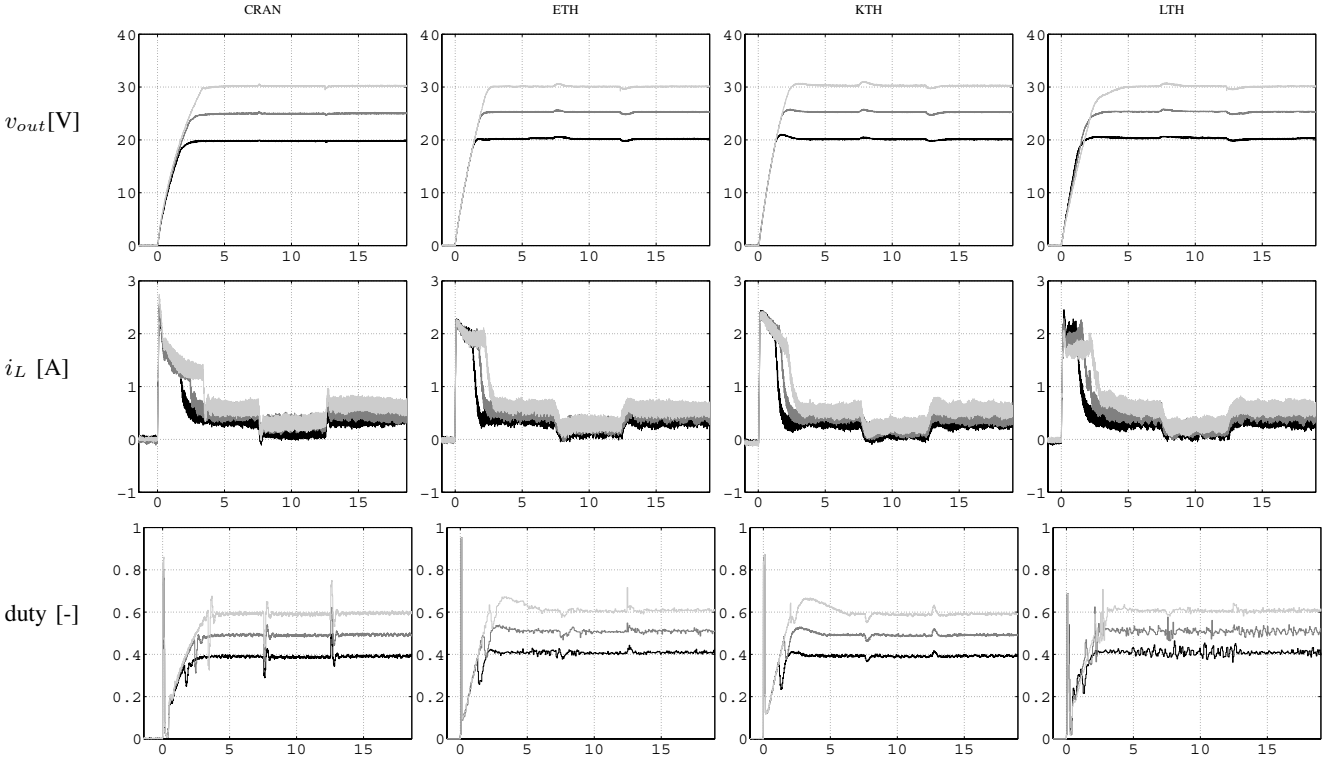


Fig. 10. Buck converter; start-up transient and response to a step in the load resistance from $r_o = 50\Omega$ to $r_o = 100\Omega$ and back again. The experiment is performed for three different values of the reference output voltage $v_{o,\mathrm{ref}}$. The values are 20V (black), 25V (gray) and 30V (light gray). The experiments of the four groups are presented side by side.

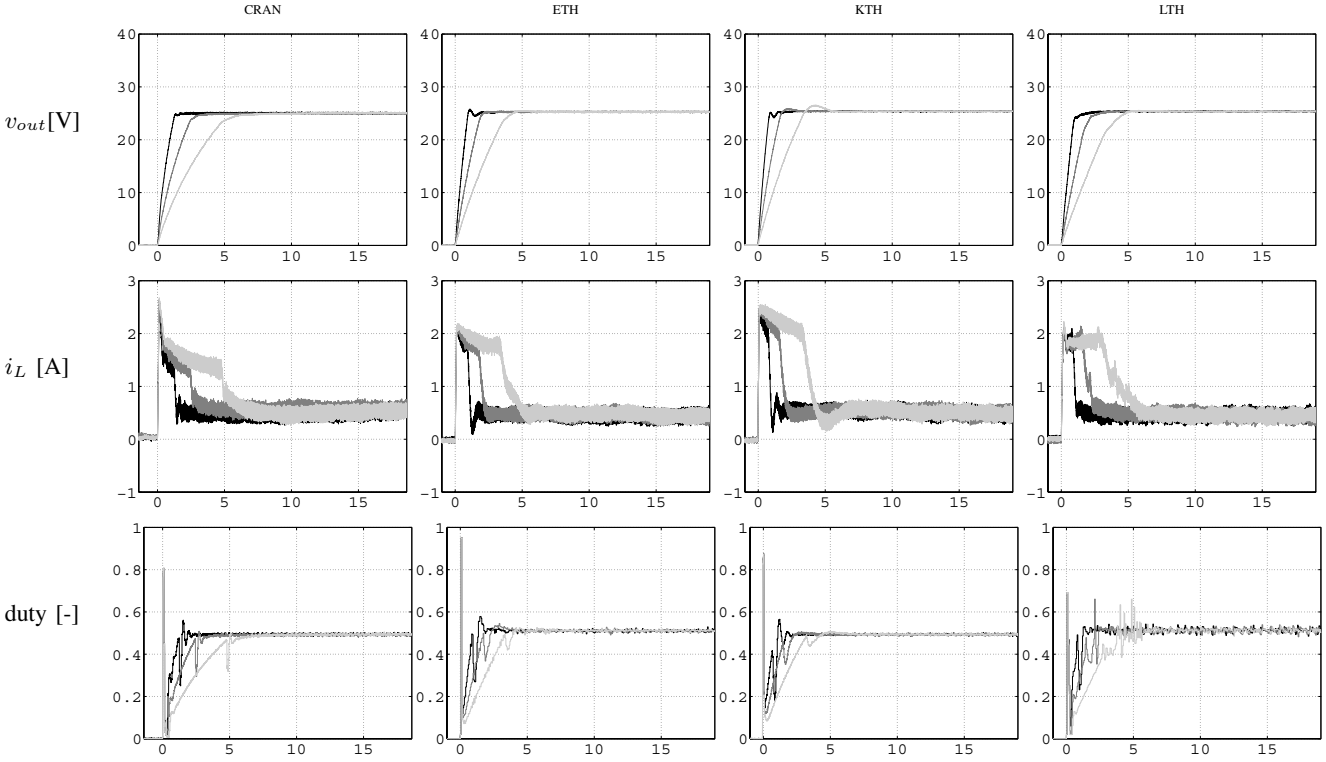


Fig. 11. Buck converter; start-up transient for three different values of the capacitance x_c (Robustness evaluation). The values are $x_c = 0.5x_{c,\mathrm{nom}}$ (black), $x_c = x_{c,\mathrm{nom}}$ (gray) and $x_c = 2x_{c,\mathrm{nom}}$ (light gray) where $x_{c,\mathrm{nom}} = 100\mu$F is the nominal value. $v_s = 50\ V$, $v_{o,\mathrm{ref}} = 25V$, $r_o = 50\Omega$. The group results are presented side by side.

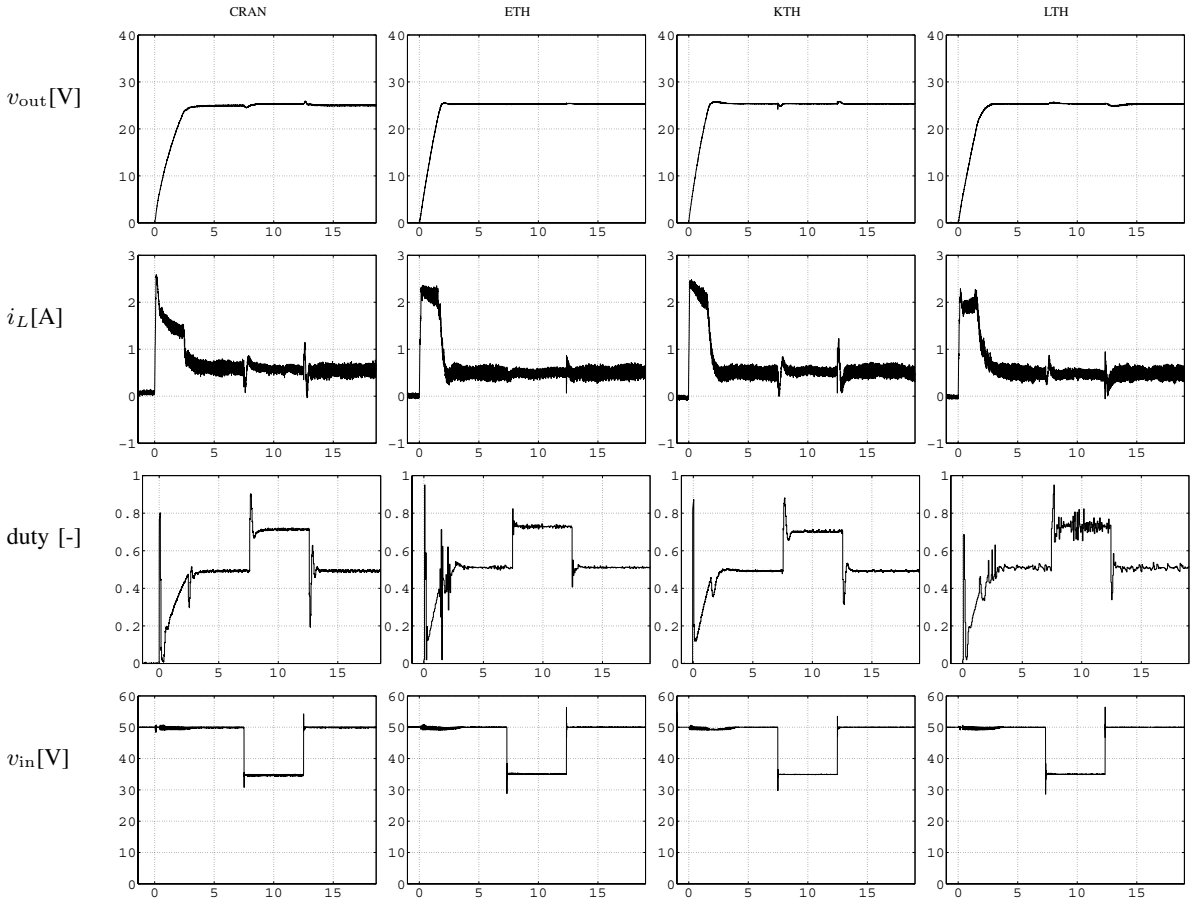


Fig. 12. Buck converter; start-up transient and response to a step in the source voltage from $v_s = 50$V to $v_s = 35$V and back again. $v_{o,\rm ref} = 25V$, $r_o = 50\Omega$.

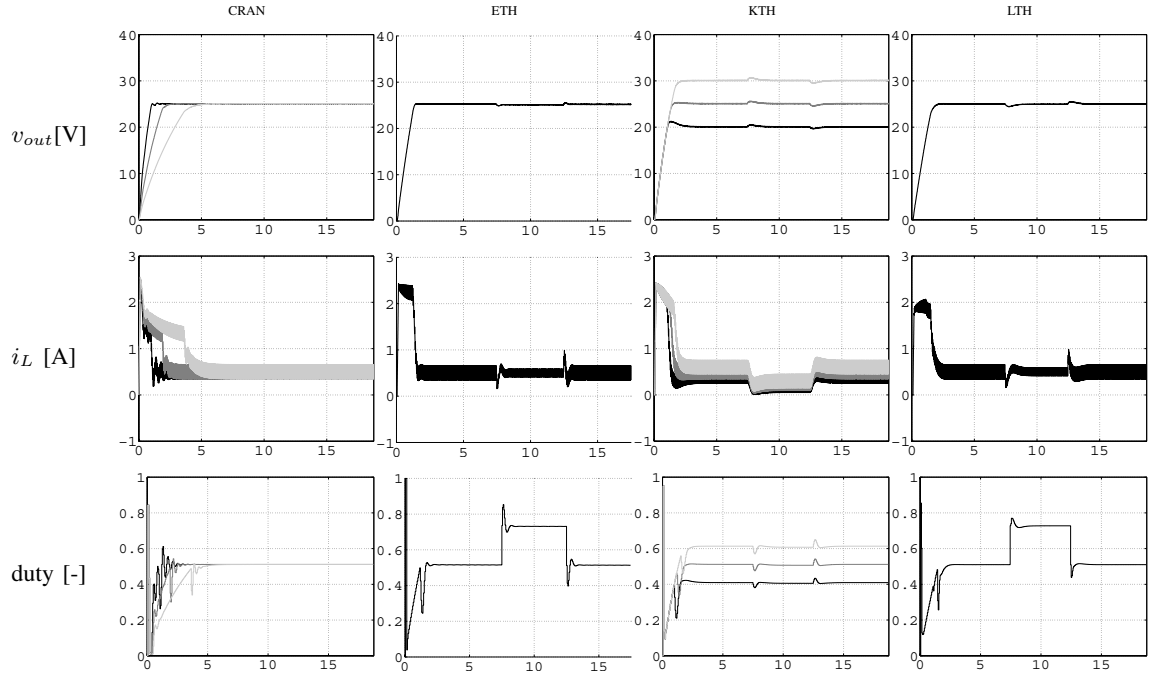


Fig. 13. Buck converter: simulation results selected for comparison with experiments. The CRAN simulation illustrates the robustness evaluation where $x_c = 50\mu$F, $x_c = 100\mu$F, and $x_c = 200\mu$F. The ETH and LTH simulations shows the start-up experiment with line transients from $v_s = 50$V to $v_s = 35$V and back again. Finally, the KTH simulation shows the start-up transient and response to a step in the load resistance from $r_o = 50\Omega$ to $r_o = 100\Omega$ and back again.

pronounced in our experimental set-up where the long wires used to access some measurements propagate noise on the control board.

5) Platform: duty cycle measurements that were obtained digitally through the DSP (ETH/LTH) also display a higher sensitivity due to the higher accuracy of the measurement and to a larger measurement bandwidth (respectively 1 MHz and 50 kHz).

6) Time available for the tuning: finally, the time available for the controller tuning was not the same for all groups due to scheduling and geographic contingencies as the experiments were all performed at ETH.

E. Experimental results evaluation for the boost topology

The experimental results that are shown in Fig. 14 to 15 are similar to the buck case. As for the buck case, the difference mostly stem from aspects not directly related to the control approach and they are not discussed further here, except for the stabilizing control approach which is also based on a different switching approach.

In this latter approach, the control variable is directly boolean and the notion of duty cycle has therefore no meaning. Nevertheless, for the sake of comparison and due to visibility issues, the evolution of the control variable is shown as an instantaneous duty ratio in Fig. 14, 15 and 16. The instantaneous duty ratio is computed off-line based on the control signal, in a similar way with the definition of the duty cycle from Section II-C. It is the ratio between the period t_{on} when the switch is on the L position, and the period $t_{on} + t_{off}$ between two consecutive commutations from H to L. As all these periods are multiples of the sampling period, the instantaneous duty ratio takes only discrete values in the interval $[0; 1]$.

For the sake of comparison some simulations were additionally performed based on the conducted experimental scenarios, although due to space limitations it was not possible to feature all cases; the simulation was carried out in Matlab^{TM}by directly using the model presented in II-C with the above nominal values and accounting for the delay due to measurement, conversion and computation. The chosen plots are displayed in Fig. 17, where in particular one scenario is presented for each controller. The first column shows the results obtained with the ETH controller for the line transient, where the simulated evolution overall mirrors the corresponding experimental sequence of values. The second column features the plots derived with the KTH controller for the load transient. Here, the simulated states correspond well with the experiment, albeit with a slightly less pronounced chattering in the duty cycle. The third column contains the simulated evolution of the LTH controller for the voltage supply variation: as previously mentioned, it is believed that the difference between simulation and experiments is due to quantization errors and noise. Finally, the last column portrays the values obtained with the SUPELEC controller for the case of varying capacitor values. The same dependence between the speed of convergence and the capacitor values can be observed. The differences observed between the simulated and the real transient and amplitude of oscillations on the current are due to the inaccuracy in the value of the physical parameters and to the measurement noise.

As a general remark, the obtained simulation results qualitatively resemble the experimental values and corroborate the validity of the proposed controller synthesis approaches, which are based on the schematic approximation of the physical circuit given in Section II-C.

VII. Conclusion

Five control methods from hybrid and optimal control have been successfully applied to fixed frequency DC-DC buck and boost converters and compared through experimentation. The various control structures presented in the paper are all based on digital control techniques where measurement and actuation takes place only at the sampling instances.

The methods presented by ETH, LTH, KTH and CRAN all act at the beginning of each switching period and use the duty cycle as the manipulated variable, rendering a constant switching frequency operation; the former two allow for a more systematic modeling of the circuit characteristics but typically yield an increased degree of complexity in the controller, whereas the third might be suitable for higher switching frequencies in view of its more affordable implementation requirements, as reflected by the associated computation times. The method of SUPELEC, on the other hand, directly decides on the discrete position of the controlled switch based on a much faster sampling of the system, and results in a scheme with an improved reaction time to disturbances, but also requires a higher measurement bandwidth and results in a variable switching frequency.

The methods described in the paper allow to impose constraints such as the limitation of the coil current, in order to avoid core saturation and to protect the semi-conductor devices. The constraints are respected either intrinsically or with the help of an external logic. In all cases, it has to be observed that some non-linear control action is necessary in order to obtain a closed loop system that respects the state and control constraints without sacrificing too much in performance.

The methods perform similarly well and display an excellent dynamic performance. Most differences that have been observed are related to the tuning of the controller or to additional control functions that are not linked to a specific approach except for SUPELEC where the faster reaction to disturbances is inherent to the direct control approach and the higher sampling frequency. The complexity of the approaches is compatible with the high-frequencies required by power electronics applications. In particular, the sampled data approach investigated by KTH is easy to implement and allows fast sampling rates to be considered. The model predictive control suggested by ETH and the relaxed dynamic programming approach by LTH allow a more systematic treatment of the non-linear design constraints but may lead to increased yet manageable complexity of the resulting controller. A linear approximation was necessary in order to implement the predictive control of CRAN and more extensive tuning than the other approaches was required. The stabilization approach

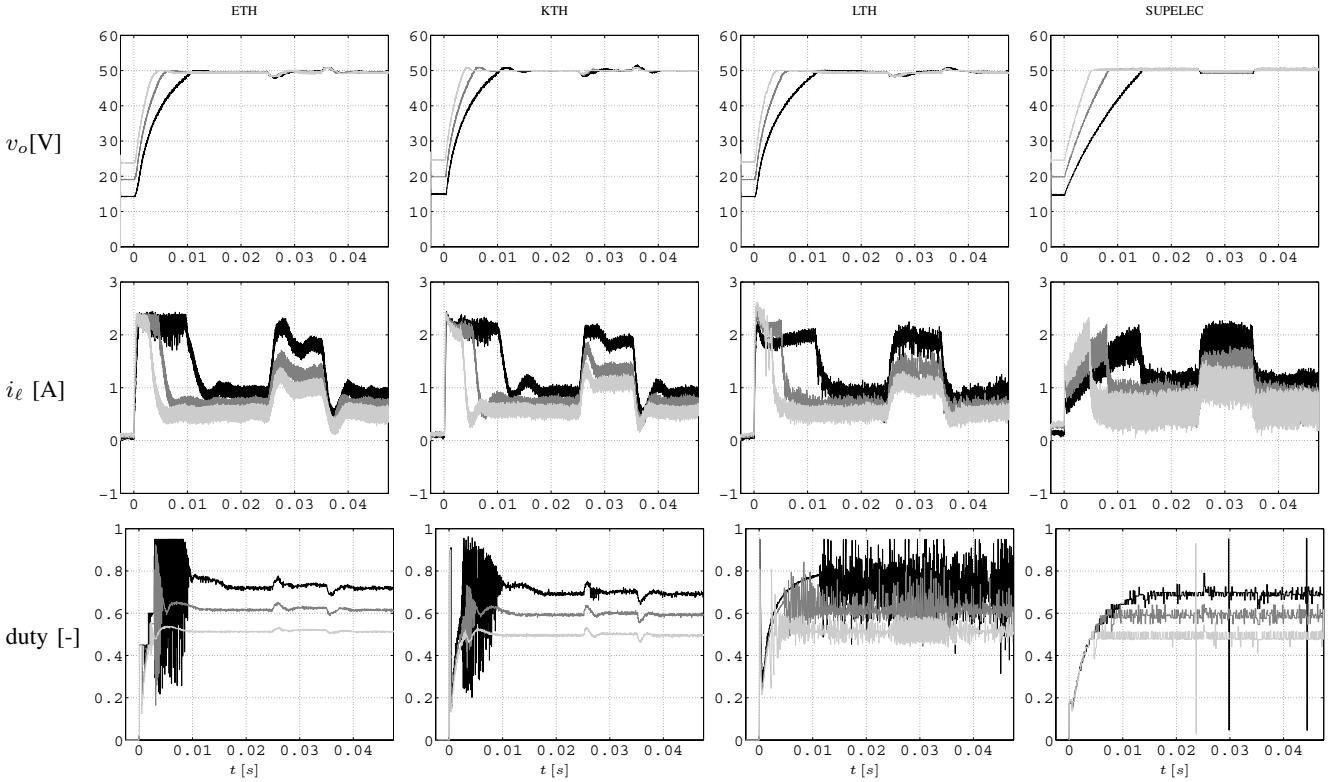


Fig. 14. Boost converter: start-up and load transient. At time t =25 ms, a load step from 200 Ω to 100 Ω is applied. At time t =35 ms a step back to the initial value is applied. v_s = 15V, 20V, 25V, $v_{o,ref}$= 50V.

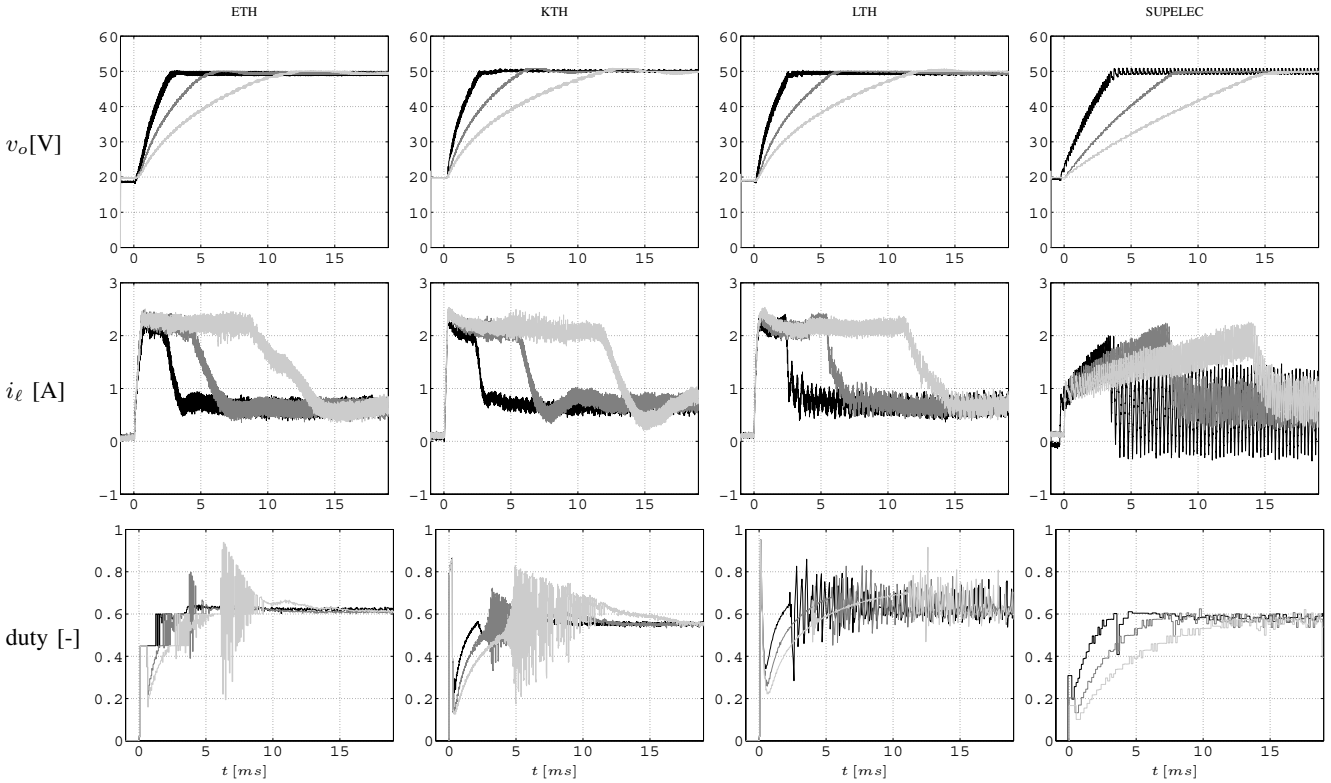


Fig. 15. Boost converter: robustness evaluation. Start-up transient for three different values of capacitor: $x_c = 50F$, $100F$, $200F$. v_s = 20V, $v_{o,\mathrm{ref}}$= 50V, $r_o = 200\Omega$

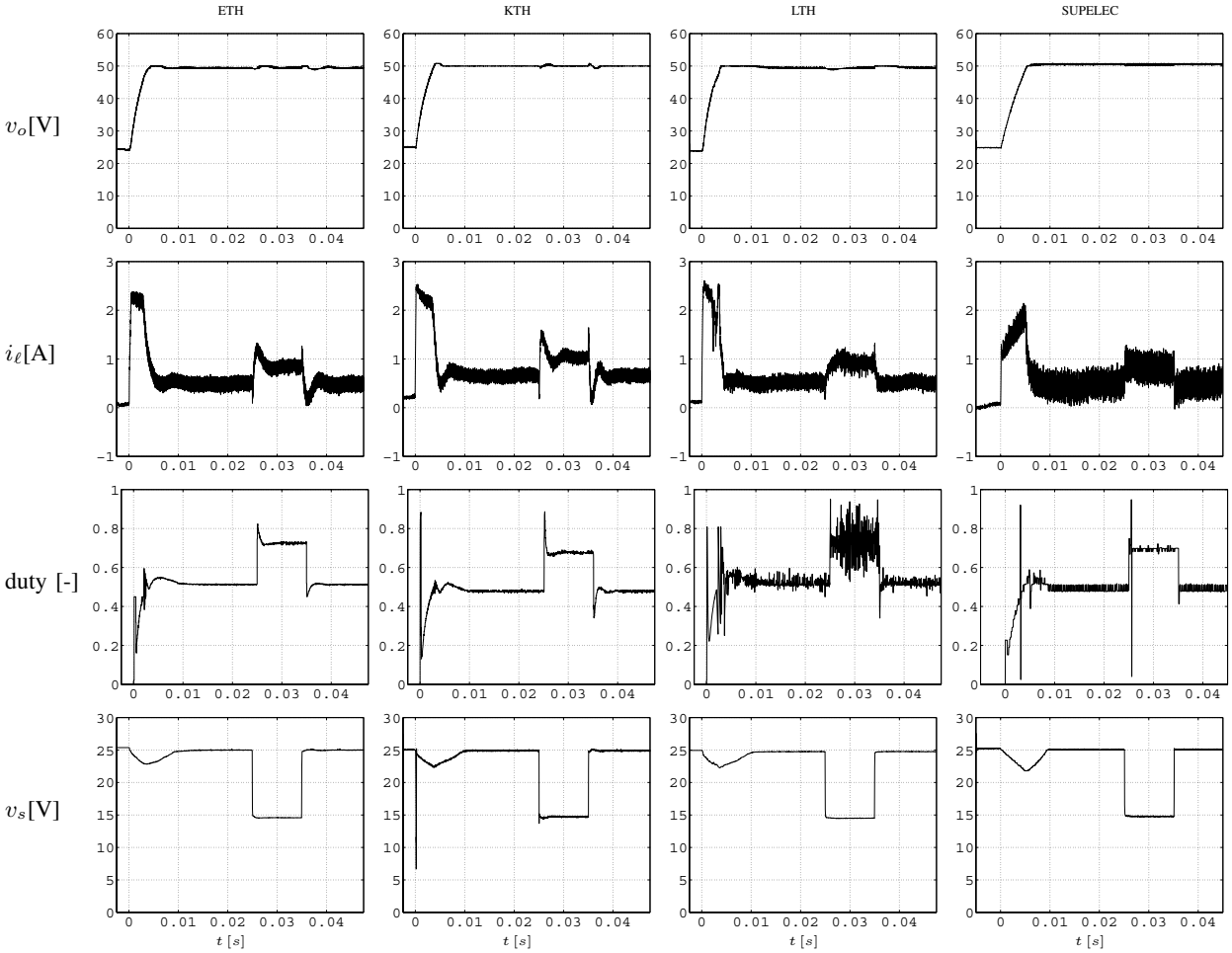


Fig. 16. Boost converter: start-up and line transient. At time t =25 ms a step-down from v_s =25V to 15V is applied on the supply voltage. At time t =35 ms a step-up to the initial value is applied. $v_{o,ref}$ = 50V, r_o = 200Ω

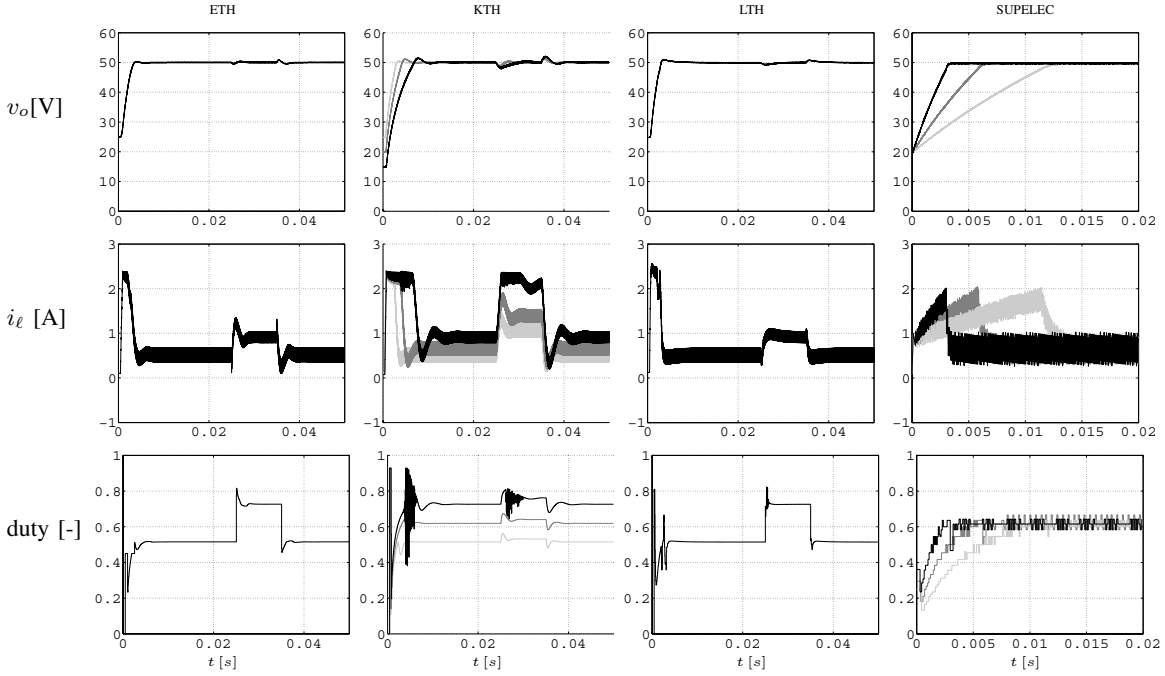


Fig. 17. Boost converter: selected simulation results for comparison with experiments.

investigated by SUPELEC required a modification in order to increased dynamic performance.

In principle, the methods can be applied in a systematic fashion to more complex control problems. Possible future directions would be to investigate how the methods can be extended to consider higher dimensional converter topologies.

In order to compare and extend the presented results to other control approaches, all relevant parameters, test scenario and corresponding Matlab simulation scripts have been made available at the following URL [41].

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