On the Optimal Control of Switch-mode DC-DC Converters

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Abstract

This paper presents a new solution approach to the optimal control problem of fixed frequency switch-mode DC-DC converters using hybrid systems methodologies. In particular, the notion of the N-step model is introduced to capture the hybrid nature of these systems, and an optimal control problem is formulated and solved online, which allows one to easily incorporate in the controller design safety constraints such as current limiting. Simulation results are provided that demonstrate the prospect of this approach.

Keywords

Power Electronics, DC-DC Converters, Model Predictive Control, Hybrid Systems

1 Introduction

Switch-mode DC-DC converters are power electronic circuits that are used in a large variety of applications due to their light weight, compact size and high efficiency and reliability. They constitute the enabling technology in computer power supplies, battery chargers, sensitive and demanding aerospace and medical applications, and variable speed DC motor drives.

Their analysis and design both in the open and the closed loop have attracted a wide research interest, and the quest for efficient control techniques is of interest for both the research and the industrial community. Because the DC voltage at the input is unregulated (consider for example the result of an AC rectification) and the output power demand changes significantly over time constituting a time-varying load, the scope is to achieve output voltage regulation in the presence of input voltage and output load variations. The difficulties in controlling DC-DC converters arise from their hybrid nature. In general, these converters feature three different modes of operation, where each mode has an associated linear continuous-time dynamic. Furthermore, constraints are present which result from the converter topology. In particular, the manipulated variable (duty cycle) is bounded between zero and one, and in the discontinuous current mode a state (inductor current) is constrained to be nonnegative. Additional constraints are imposed as safety measures, such as current limiting or soft-starting, where the latter constitutes a constraint on the maximal derivative of the current during start-up. The control problem is further complicated by

gross operating point changes due to input voltage and output load variations, and model uncertainties.

Fixed-frequency switch-mode DC-DC converters are switched circuits that transfer power from a DC input to a load. Using a semiconductor switch that is periodically switched on and off and a low-pass filtering stage with an inductor and a capacitor, a DC voltage with a small ripple is produced at the output. The switch is driven by a pulse sequence that has a constant frequency (period), the *switching frequency* f_s (*switching period* T_s), which characterizes the operation of the converter. The DC component of the output voltage can be regulated through the duty cycle d that is defined by $d = \frac{t_{on}}{T_s}$, where t_{on} represents the interval within the switching period during which the switch is in conduction.

The main approach to model DC-DC converters is the method of state-space averaging [19, 4]. In order to bypass the difficulties posed by the hybrid nature of the system, an averaged continuous-time model is obtained that uses the duty cycle as an input and describes the system's slow dynamics. The result of this procedure is still a nonlinear model due to the presence of multiplicative terms involving the state variables and the duty cycle. The controller design is carried out using linear control techniques for a model linearized around a specific operating point. Apart from the limitations of this approximation, the averaging procedure hides all information about the fast dynamics of the system, and fast instabilities like subharmonic oscillations are not captured. A more rigorous approach is to describe the system with discrete-time models that map the state variables from the beginning to the end of the switching period [11, 14]. These methods successfully describe many aspects of the complex DC-DC converters' dynamics and are very suitable for analyzing phenomena like subharmonic and chaotic oscillations that have been observed when DC-DC converters operate in closed loop [8]. Nevertheless, for design purposes they still carry the basic disadvantage of being nonlinear with respect to the duty cycle, and therefore do not always offer a systematic approach to the controller design problem.

The main control objective for DC-DC converters is to drive the semiconductor switch with a duty cycle such that the DC component of the output voltage is equal to its reference. This regulation needs to be maintained despite variations in the load or the input voltage. The basic concept that is currently used for the control of DC-DC converters is the Pulse Width Modulation (PWM): The switch is turned on at the beginning of each switching period, and it is turned off by the controller when a certain condition is fulfilled. A latch keeps the switch turned off until the beginning of the next period. With this formulation, the control problem is to decide at which instant within the switching period the switch should be turned off.

In practice a variety of different control strategies are used, categorized in voltage and current mode control schemes [20]. They are all PI-type controllers tuned based on the above linearized average models. Simple rules, such as selecting a cross-over frequency an order of magnitude smaller than the switching frequency and a phase margin in the range of 45 to 60 degrees are used. Depending on the converter topology and the control strategy selected, these tuning

guidelines result in step responses with typical overshoots of up to five percent and settling times in the range of $5 - 30$ switching periods.

In the literature a wide range of different strategies has been proposed for improved controller design. The methods introduced vary from Fuzzy Logic [7] to Linear Quadratic Regulators (LQR) [15, 16, 5], and from non-linear control techniques [21, 22, 9] to feedforward control [12, 13]. The common element in all these approaches is the use of simplified models for the description of the dynamic behavior of switch-mode DC-DC converters. It is obvious that approximations like the use of averaged or locally linearized models do not allow to capture the complex dynamics that stem from the hybrid nature of DC-DC converters, and unavoidably narrow the space of the explored phenomena producing results of limited validity. In particular, for the LQR design in [15, 16] discrete-time models linearized around an operating point are used, and for the nonlinear design in [21, 22, 9] the hybrid nature of the DC-DC converters is bypassed by using an averaged model for the controller design. Furthermore, none of the proposed controllers allows to address the issue of constraints in the design procedure. In more recent work, the hybrid nature of DC-DC converters is addressed for modelling and controller design [23, 17].

Motivated by these difficulties, we present in this paper a novel approach to the modelling and controller design problem for DC-DC converters, using a synchronous step-down DC-DC converter as an illustrative example. The converter is modelled as a hybrid system using the Mixed Logic Dynamic (MLD) [2] framework. This leads to a model that is valid for the whole operating regime and captures the evolution of the state variables within the period. Based on the MLD model, we formulate and solve a finite time optimal control problem. This results in a systematic controller design that achieves the objective of regulating the output voltage to the reference despite input voltage and output load variations while satisfying the constraints. In particular, the control performance does not degrade for changing operating points.

The paper is organized in the following way: In Section 2, the synchronous step-down converter is modelled in the MLD framework by introducing the notion of the N-step model. In Section 3, an optimal control problem incorporating the above mentioned control objectives is formulated. Simulation results illustrating various aspects of the system's behavior are given in Section 4. Finally, conclusions and further research directions are discussed in Section 5.

2 Modelling the Synchronous Converter

We start by modelling the synchronous step-down converter in continuous-time, and derive for each mode of operation the state-space equations. The model incorporates the parasitic elements, in particular the internal resistance of the inductor and the Equivalent Series Resistance (ESR) of the capacitor.

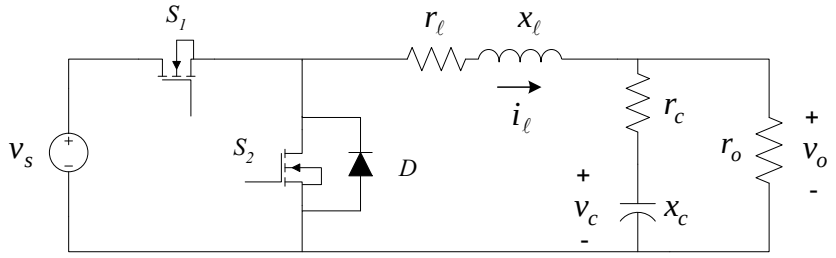


Fig. 1. Topology of the step-down synchronous converter

2.1 Continuous-Time Model

The circuit topology of the synchronous step-down converter is shown in Fig. 1. Using normalized quantities, r_o denotes the output load which we assume to be ohmic, r_c the ESR of the capacitor, r_ℓ is the internal resistance of the inductor, x_ℓ and x_c represent the inductance and the capacitance of the low-pass filtering stage, and v_s denotes the input voltage. For every period k, a duty cycle $d(k)$ which is bounded between zero and one is chosen by the controller. For the time interval $kT_s \leqslant t < (k + d(k))T_s$ the switch S_1 is conducting and power is transferred from the input directly to the load. While S_1 is on, the switch S_2 is off and the diode D is reversed biased. At the end of this interval, S_1 is turned off and kept off until the beginning of the next cycle. The switch S_2, which operates dually with respect to S_1, is turned on for $(k+d(k))T_s \leqslant t < (k+1)T_s$. Together with the diode D, the switch S_2 provides a path for the inductor's current i_ℓ regardless whether the latter is positive or negative.

Defining $x(t) = [i_\ell(t)\ v_c(t)]^T$ as the state vector, where $i_\ell(t)$ is the inductor current and $v_c(t)$ the capacitor voltage, and given the duty cycle $d(k)$ during the k-th period, the system is described by the following set of affine continuous-time state-space equations. While S_1 is conducting, they amount to

$$\dot{x}(t) = Fx(t) + fv_s, \quad kT_s \leqslant t < (k + d(k))T_s, \tag{1}$$

and if S_1 is off, the system evolves autonomously, i.e.

$$\dot{x}(t) = Fx(t), \quad (k + d(k))T_s \leqslant t < (k + 1)T_s. \tag{2}$$

where the matrices F and f are given by

$$F = \begin{bmatrix} -\frac{1}{x_\ell}(r_\ell + \frac{r_o r_c}{r_o+r_c}) & -\frac{1}{x_\ell}\frac{r_o}{r_o+r_c} \\ \frac{1}{x_c}\frac{r_o}{r_o+r_c} & -\frac{1}{x_c}\frac{1}{r_o+r_c} \end{bmatrix}, \quad f = \begin{bmatrix} \frac{1}{x_\ell} \\ 0 \end{bmatrix}. \tag{3}$$

The output voltage $v_o(t)$ across the load r_o is expressed as a function of the states through

$$v_o(t) = g^T x(t) \tag{4}$$

with

$$g = \left[\frac{r_o r_c}{r_o + r_c} \; \frac{r_o}{r_o + r_c} \right]^T . \tag{5}$$

The output variable which is of main interest from a control point of view, however, is the output voltage error which is obtained by integrating the difference between the output voltage and its reference over the k-th switching period, i.e.

$$v_{o,err}(k) = \int_{kTs}^{(k+1)Ts} (v_o(t) - v_{o,ref})\, dt, \tag{6}$$

where $v_{o,ref}$ denotes the reference of the output voltage.

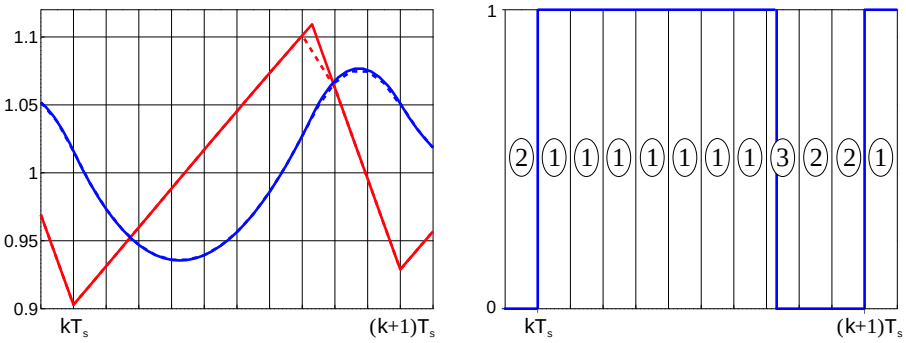
Summing up, the synchronous converter features two operation modes with two different affine dynamics. Both modes differ only in the affine expression and have the same output function. At the beginning of each period, always the first mode with (1) is active. The duty cycle $d(k)$ determines the transition time from the first to the second mode which evolves according to (2).

It is important to note that in current practice the inductor current $i_\ell(k)$ and the output voltage $v_o(k)$ can be directly measured. Based on these two measurements, the second state $v_c(k)$ can be easily computed. Alternatively, given the fact that the capacitor's ESR is very small, assuming that the capacitor voltage $v_c(k)$ is equal to the output voltage $v_o(k)$ at the sampling instants k introduces only a small error. Variations in the input voltage v_s are also considered to be measurable in accordance with common practice [20].

The constraints that are present in the converter model come from two different sources. By definition, the duty cycle $d(k)$ is constrained between zero and one. The fact that the semiconductor devices and the load can physically handle only a certain maximal current poses an additional upper bound on the inductor current, given by $i_\ell(t) < i_{\ell,max}$. This constraint is known as the current limit and is application specific.

2.2 *N*-step Discrete-Time Hybrid Model

The goal of this section is to derive a model of the synchronous step-down converter that is suitable as a prediction model for the optimal control problem which we will formulate in the Section 3. This model should include the following properties. First, it is natural to formulate the model and the controller in the discrete-time domain, as the manipulated variable given by the duty cycle is constant within a period T_s and changes only at every time-instant kT_s, $k \in \mathbb{N}$. Second, it would be beneficial to capture the evolution of the states also within one period, as this would enable us to impose constraints not only on the states at time-instants kT_s but also on intermediate values. This is particularly important for the inductor current which can vary drastically within one period and would allow us to keep its peaks below the current limit. Third, the model needs to yield an approximation of the output voltage error. Most important, as the converter is intrinsically hybrid in nature, we aim to retain the structure of the two operation modes and account for the hybrid character.



(a) Evolution of the states

(b) Position of the switch S_1 and the number of the mode which is active in the respective subperiod

Fig. 2. The N-step modelling approach visualized for the k-th period. The evolution of the states of the continuous-time nonlinear model (solid lines) is compared with the sequence of states of the discrete-time hybrid model (dashed lines) using $N = 10$ subperiods, where the saw tooth shaped line represents i_ℓ and the smooth curve is v_c.

Motivated by these considerations, we introduce the N-step modelling approach that accounts for all the above requested properties by dividing the period of length T_s into N *subperiods* of length $\tau_s = T_s/N$ with $N \in \mathbb{N}$, $N \geq 2$. This concept is illustrated in Fig 2. We denote the states within a subperiod sampled with τ_s by $\xi(n)$, and we refer to the discrete time-instants of the subperiods by n, where $n \in \{0, 1, \ldots, N-1\}$. Furthermore, by definition, $\xi(0) = x(k)$ and $x(k+1) = \xi(N-1)$ hold.

Next, we introduce N binary variables

$$\sigma_n = \text{true} \iff d(k) \geq \frac{n}{N}, \qquad n = 0, \ldots, N-1 \tag{7}$$

which represent the sampled switch position of S_1 at time-instants $n\tau_s$. Recall that the switch S_2 is dually operated with respect to S_1.

For each subperiod, we introduce the two modes discussed above (switch closed and open, respectively) plus an additional third mode that captures the transition from mode 1 to 2. More specifically, the modes are (i) the switch S_1 remains closed for the whole subperiod, (ii) the switch S_1 is open for the whole subperiod, and (iii) the switch S_1 is opening within the subperiod. Hence, for the n-th subperiod, the state-update equations amount to

$$\xi(n+1) = \begin{cases} \Phi\, \xi(n) + \Psi, & \text{if } \sigma_n \ \wedge \ \sigma_{n+1}, \\ \Phi\, \xi(n), & \text{if } \bar{\sigma}_n, \\ \Phi\, \xi(n) + \Psi(Nd(k) - n), & \text{if } \sigma_n \ \wedge \ \bar{\sigma}_{n+1}, \end{cases} \tag{8}$$

where Φ and Ψ are the discrete-time representations of F and f as defined in (3) with sampling time τ_s. The third (auxiliary) mode refers to the mode transition

where the switch S_1 opens within a subperiod. Note that if we are in the third mode, i.e. $\sigma_n \ \wedge \ \bar{\sigma}_{n+1}$ holds, $Nd(k) - n$ is bounded by zero and one. Thus, the third mode constitutes a weighted average of modes one and two. The error introduced by averaging can be made arbitrarily small by increasing N.

Using the sampled output voltage given by

$$v_o(n) = g^T \ \xi(n), \tag{9}$$

we approximate the voltage error integral (6) for the k-th period in the following way.

$$v_{o,err}(k) = \sum_{n=0}^{N-2} \frac{v_o(n) + v_o(n+1)}{2(N-1)} - v_{o,ref} \tag{10}$$

In summary, the N-step modelling approach provides a description of the state evolution within one period. In particular, the discrete-time sequence of $\xi(n)$, $n = 0, \ldots, N-1$ is an accurate sampled representation of the continuous-time evolution of $x(t)$ for $t \in [kT_s, (k+1)T_s]$. The only approximation that has been introduced appears in the third mode of (8) when the switch S_1 is turned off.

2.3 MLD Framework

The three operation modes of the N-step model call for appropriate modelling using hybrid methodologies. As basically all discrete-time hybrid modelling schemes can be transformed into each other, we employ the Mixed Logical Dynamic (MLD) framework as it allows for convenient modelling using HYSDEL (HYbrid System DEscription Language) [24], and it is well-suited for optimal control, namely Model Predictive Control (MPC) computations. In particular, efficient conversion tools are available [6] to transform MLD models into piecewise affine (PWA) models. A PWA representation will be needed at a later stage to precompute offline the MPC feedback law for the whole state space that renders the optimal controller applicable for online implementations with sampling times in the range of several μs [3].

The general MLD form of a hybrid system introduced in [2] is

$$x(k+1) = Ax(k) + B_1 u(k) + B_2 \delta(k) + B_3 z(k) \tag{11a}$$

$$y(k) = Cx(k) + D_1 u(k) + D_2 \delta(k) + D_3 z(k) \tag{11b}$$

$$E_2 \delta(k) + E_3 z(k) \leq E_4 x(k) + E_1 u(k) + E_5, \tag{11c}$$

where $k \in \mathbb{N}$ is again the discrete time-instant, and $x \in \mathbb{R}^{n_c} \times \{0,1\}^{n_\ell}$ denotes the states, $u \in \mathbb{R}^{m_c} \times \{0,1\}^{m_\ell}$ the inputs and $y \in \mathbb{R}^{p_c} \times \{0,1\}^{p_\ell}$ the outputs, with both continuous and binary components. Furthermore, $\delta \in \{0,1\}^{r_\ell}$ and $z \in \mathbb{R}^{r_c}$ represent binary and auxiliary continuous variables, respectively. These variables are introduced when translating propositional logic or PWA functions into linear inequalities. All constraints on states, inputs and auxiliary variables are summarized in the inequality (11c). Note that the equations (11a) and (11b)

are linear; the nonlinearity is hidden in the integrality constraints over the binary variables. We consider MLD systems that are *completely well-posed* [2], i.e. for given $x(k)$ and $u(k)$, the values of $\delta(k)$ and $z(k)$ are uniquely defined by the inequality (11c). This assumption is not restrictive and is always satisfied when real plants are described in the MLD form [2].

The above procedure yields an MLD system with two states, $7N + 3$ z-variables, N δ-variables and $24N + 18$ inequality constraints. The derivation of the MLD system is performed by the compiler HYSDEL generating the matrices of the MLD system starting from a high-level description of the system.

3 Optimal Control

3.1 Model Predictive Control

Model Predictive Control (MPC) has been used successfully for a long time in the process industry and recently also for hybrid systems. As shown in [2], MPC is well suited for the control of hybrid systems described in the MLD framework. The control action is obtained by minimizing an objective function over a finite or infinite horizon subject to the mixed-integer linear inequality constraints of the MLD model (11) and the physical constraints on the manipulated variables. Depending on the norm used in the objective function, this minimization problem amounts to solving a *Mixed-Integer Linear Program* (MILP) or *Mixed-Integer Quadratic Program* (MIQP).

The major advantage of MPC is its straight-forward design procedure. Given a (linear or hybrid) model of the system, one only needs to set up an objective function that incorporates the control objectives. Additional hard (physical) constraints can be easily dealt with by adding them as inequality constraints, whereas soft constraints can be accounted for in the objective function using penalties. For details concerning the set up of the MPC formulation in connection with MLD models, the reader is referred to [2] and [1]. Details about MPC can be found in [18].

3.2 Optimal Control Problem

The control objectives are to regulate the average output voltage to its reference as fast and with as little overshoot as possible, or equivalently, to minimize the output voltage error $v_{o,err}(k)$, despite changes in the input voltage v_s or changes in the load resistance r_o, and to respect the constraint on the inductor current. Let

$$\Delta d(k) = d(k) - d(k-1) \tag{12}$$

denote the difference between two consecutive duty cycles. To allow for aggressive control moves when the voltage error is large but to force the controller to act cautiously if the output voltage is close to the reference and the voltage error is small, we penalize a saturated version of $\Delta d(k)$ using the variable

$$\varepsilon_d(k) = \begin{cases} \Delta d(k), & \text{if } |\Delta d(k)| \leq \Delta d_{max}, \\ \Delta d_{max}, & \text{else} \end{cases} \tag{13}$$

rather than $\Delta d(k)$ directly. To account for the bound $i_{\ell,max}$ on the inductor current, we introduce the variable $\varepsilon_i(k)$ that describes the degree of the violation of this constraint.

$$\varepsilon_i(k) = \begin{cases} 0, & \text{if } i_\ell(k) \leq i_{\ell,max}, \\ i_\ell(k) - i_{\ell,max}, & \text{else} \end{cases} \tag{14}$$

By associating a large penalty weight with $\varepsilon_i(k)$, the upper bound on the inductor current is modelled as a soft constraint. Note that for (14) an additional binary variable is not needed as it can be represented by a slack variable.

Define the penalty matrix $Q = \text{diag}(q_1, q_2, q_3)$ with $q_1, q_2, q_3 \in \mathbb{R}^+$ and the vector $\varepsilon(k) = [v_{o,err}(k),\ \varepsilon_d(k),\ \varepsilon_i(k)]^T$, with $v_{o,err}(k)$ as defined in (10). Consider the objective function

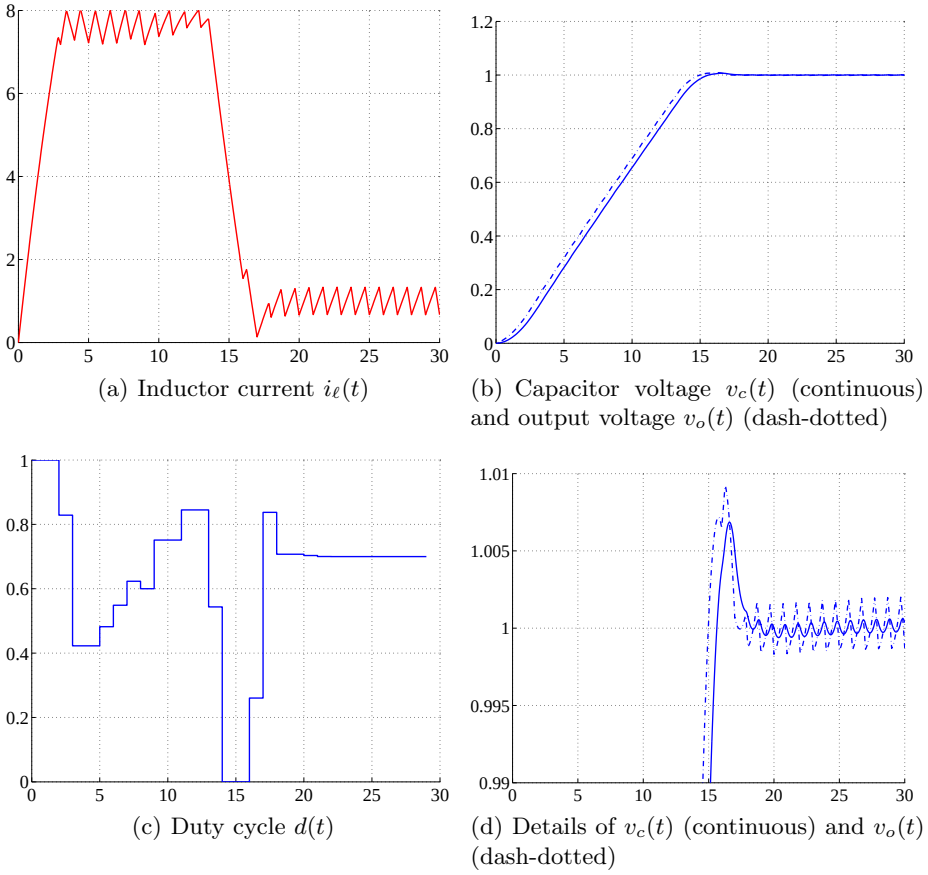
$$J(D(k), x(k), d(k-1)) = \sum_{\ell=0}^{L-1} \|Q\ \varepsilon(k+\ell|k)\|_1 \tag{15}$$

which penalizes the predicted evolution of $\varepsilon(k+\ell|k)$ from time-instant k on over the finite horizon L using the 1-norm. The control law at time-instant k is then obtained by minimizing the objective function (15) over the sequence of control moves $D(k) = [d(k), \ldots, d(k+L-1)]^T$ subject to the mixed-integer linear inequality constraints of the MLD model (11), the physical constraint on the duty cycle $d(k) \in [0, 1]$, and the expressions (12)-(14). As we are using the 1-norm, this minimization problem is a *Mixed-Integer Linear Program* (MILP) for which efficient solvers exist.

4 Simulation Results

In this section, simulation results demonstrating the potential advantages of the proposed control methodology are presented. The circuit parameters used in the simulations were chosen to represent a realistic problem set-up, describing for example a 48 V to 32 V, 100 W step-down DC-DC converter. Expressed in the per unit system, they are given by $x_c = 600\,\text{p.u.}$, $x_\ell = 3\,\text{p.u.}$, $r_c = 0.005\,\text{p.u.}$ and $r_\ell = 0.05\,\text{p.u.}$ If not otherwise stated, the output resistance is given by $r_o = 1\,\text{p.u.}$ and the output voltage reference is $v_{o,ref} = 1$.

The four cases included here represent different scenarios that are of interest in practical applications and pose performance challenges for any control scheme. In all cases, the current limit for the converter has been set to $i_{\ell,max} = 8\,\text{p.u.}$ The penalty matrix is chosen to be $Q = \text{diag}(5, 1, 1000)$, putting a rather small weight on the changes of the manipulated variable and a very large penalty on the violation of the current limit. Furthermore, the saturation limit for the maximal cost on the changes in the control moves is chosen as $\Delta d_{max} = 0.02$. The prediction horizon in all cases is $L = 4$. Although even 10 subperiods yield very accurate results, $N = 20$ subperiods are chosen for the N-step model to very accurately model the nonlinear dynamics. All the simulation results presented



(a) Inductor current $i_\ell(t)$

(b) Capacitor voltage $v_c(t)$ (continuous) and output voltage $v_o(t)$ (dash-dotted)

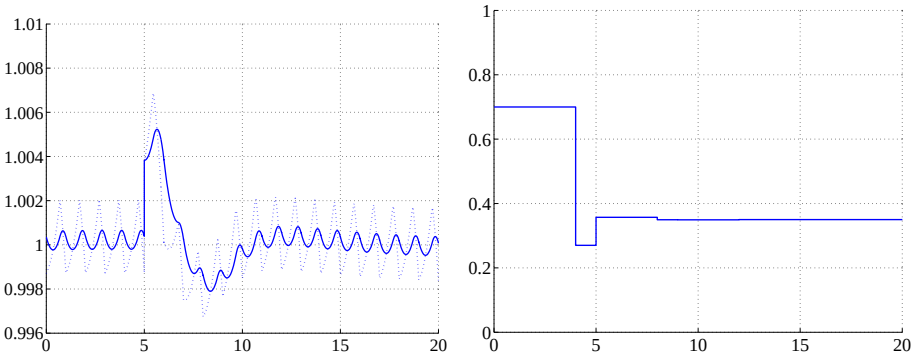
(c) Duty cycle $d(t)$

(d) Details of $v_c(t)$ (continuous) and $v_o(t)$ (dash-dotted)

Fig. 3. Step response of the converter in nominal operation

in the following figures are normalized, including the time scale where one time unit is equal to one switching period.

The first case presented in Fig. 3 shows the step response of the converter in nominal operation during start-up. The initial state is given by $x(0) = [0,\ 0]^T$, the input voltage is $v_s = 1.5\,\text{p.u.}$ and the reference for the output is $v_{o,ref} = 1\,\text{p.u.}$ The current constraint is respected by the peaks of the inductor current during start-up, and the output voltage reaches its steady state within 15 switching periods with practically no overshoot. As mentioned in the introduction, settling times of up to 30 periods and overshoots of 5 percent are commonly encountered when using PI-type controllers. The difference between the ripples of the capacitor and the input voltages is due to the presence of the ESR of the capacitor and is an inherent characteristic of switch-mode DC-DC converters. This also holds for the ripple that is observed in the inductor current.



(a) Capacitor voltage $v_c(t)$ (continuous) and output voltage $v_o(t)$ (dotted)

(b) Duty cycle $d(t)$

Fig. 4. Response of the converter to a step change in the input voltage from $v_s = 1.5\,\text{p.u.}$ to $v_s = 3\,\text{p.u.}$ at time-instant $k = 4$

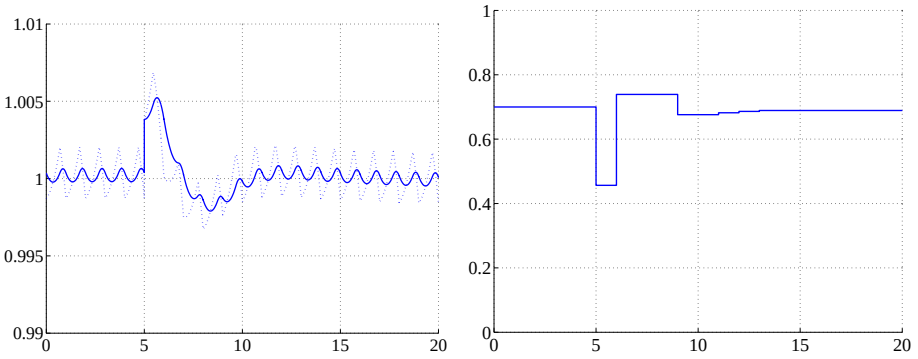
In the second case, the converter is initially at steady state when a step change in the input voltage from $v_s = 1.5\,\text{p.u.}$ to $v_s = 3\,\text{p.u.}$ is applied at time-instant $k = 4$. As can be seen from Fig. 4, the output voltage remains practically unaffected and the controller finds the new steady state duty cycle very quickly. This new duty cycle is also responsible, due to the open-loop characteristics of the converter, for a larger ripple in the inductor current. For such a rapid response to be possible, the input voltage v_s is considered to be measurable and fed to the controller. This technique is also used in current practice, where v_s is measured and used in feed-forward schemes in order to achieve faster output voltage regulation with respect to input voltage changes [20].

In the following two cases, the response of the converter to output load changes is addressed. The load resistance r_o can vary significantly over time, featuring both slow changes and step changes. Since the controller is designed through a model-based approach, it is important that some estimation procedure is employed in order to update the model used for the online optimization. The basic concept of such a scheme is briefly outlined here.

Given the measured states at time-instants $k-1$ and k, and the duty cycle at time $k-1$, we observe the following. Firstly, for a given combination of states $x(k-1)$, duty cycle $d(k-1)$ and load resistance $r_o(k-1)$ at time-instant $k-1$, computing the states at time-instants k is straightforward and involves only matrix multiplications. We refer to these states as *predicted* states $\hat{x}(k|k-1)$ using $r_o(k-1)$. Secondly, it can be shown that, when varying $r_o(k-1)$, the 2-norm of the difference between the measured and the predicted states

$$||x(k) - \hat{x}(k|k-1)||_2 \tag{16}$$

is quasi-convex in $r_o(k-1)$. Thus we can employ standard bisection optimization techniques to minimize (16). This yields at time-instant k the estimate $\hat{r}_o(k-1)$



(a) Capacitor voltage $v_c(t)$ (continuous) and output voltage $v_o(t)$ (dotted)

(b) Duty cycle $d(t)$

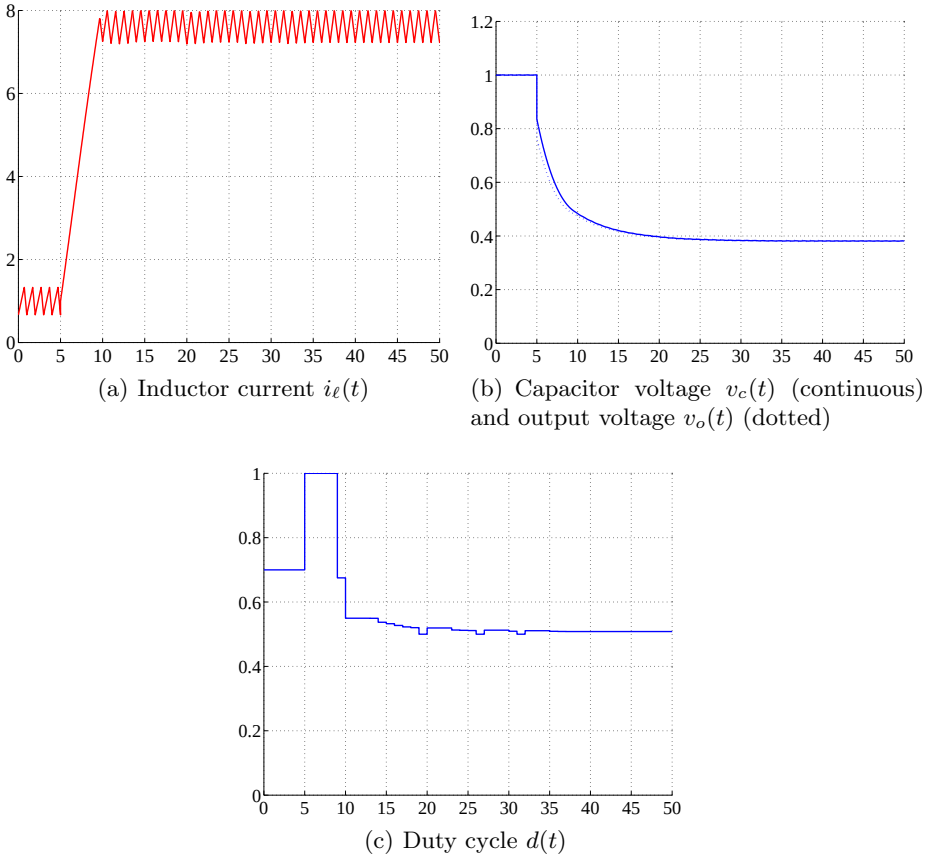
Fig. 5. Response of the converter to a step change in the load resistance from $r_o = 1\,\text{p.u.}$ to $r_o = 1.5\,\text{p.u.}$ at time-instant $k = 4$

of the load resistance. Such an estimator scheme works well if the measurement noise and the model uncertainties are negligible as is the case here. In general, however, the load resistor estimates need to be further processed and smoothed (for example by a low-pass filter) making the use of an extended Kalman filter preferable [10].

Employing the above described estimation scheme, the response of the converter to a step change in the output load is presented in Fig. 5. Starting from the steady state, the load steps up at time-instant $k = 4$ from $r_o = 1\,\text{p.u.}$ to $r_o = 1.5\,\text{p.u.}$ The new parameter for the output resistance is estimated within one switching period after the step change, and the model used for the optimal control problem is updated accordingly. As can be seen from both the current and the voltage responses, this disturbance is rejected very effectively by the controller, and the output voltage is quickly restored to the reference.

In the last case, we examine a crucial aspect of the controller operation, namely the system's protection against excessive load currents. The load drops at $k = 4$ from its nominal value to a very small one (namely to $r_o = 0.05$), almost creating a short circuit at the output. The simulation results in Fig. 6 show that the controller respects the current limit and forces the output voltage to drop to the level that is needed in order to keep the current bounded.

This example shows that the two control objectives *minimize the output voltage error* and *respect the constraint on the inductor current* are potentially contradicting each other. By putting a very large penalty on the violation of the soft constraint, we have prioritized these objectives making sure that the latter objective is always fulfilled and the converter is not destroyed by excessive current. Such a feature is utilized in all practical applications through various protection schemes, but is usually not considered as part of the controller design.



(a) Inductor current $i_\ell(t)$

(b) Capacitor voltage $v_c(t)$ (continuous) and output voltage $v_o(t)$ (dotted)

(c) Duty cycle $d(t)$

Fig. 6. Response of the converter to a step change in the load resistance from $r_o = 1\,\text{p.u.}$ to $r_o = 0.05\,\text{p.u.}$ at time-instant $k = 4$

5 Conclusions and Outlook

In this paper, we have presented a new solution approach to the optimal control problem of fixed frequency switch-mode DC-DC converters using hybrid systems methodologies. A novel N-step model was introduced to capture the hybrid nature of these systems within one switching period, and an optimal control problem was formulated and solved online. The use of MPC has allowed us to explicitly take into account during the controller design physical constraints, such as the restriction of the duty cycle between zero and one, and safety constraints, such as current limiting. Simulation results have been provided which demonstrate that this approach leads to a closed-loop system with very favorable dynamical properties.

This study has been limited to the case where the state-updates and the proposed load estimation scheme are considered to be ideal. These assumptions rep-

resent shortcomings that in the course of further research need to be addressed. In particular, the robustness of the proposed control scheme with respect to model uncertainties and measurement noise, and the asymptotic stability of the closed-loop system need to be investigated. Furthermore, the online solution of the optimal control problem requires computation times that are well above the sampling times used in real-life applications. Therefore, the experimental verification of the foreseen benefits of the proposed approach also requires the computation of the optimal state-feedback control law parameterized over the state space. This operation reduces the online optimization involving MILPs to a simple search in a look-up table requiring only matrix multiplications.

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