Deadlock Avoidance in Model Predictive Direct Torque Control

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***Abstract*—For medium voltage AC drives, model predictive direct torque control (MPDTC) shows excellent performance characteristics regarding the switching frequency and the harmonic distortion of the torque and the stator currents, outperforming classic control schemes, such as direct torque control (DTC) and field oriented control. Besides these advantages, the MPDTC algorithm runs occasionally into so called deadlocks, in which no suitable voltage vector exists, similar to DTC. Even though an exit strategy is available to resolve these situations, deadlocks tend to cause spikes in the instantaneous switching frequency and impact the overall performance of MPDTC. This paper focuses on new methods to avoid such deadlocks, using terminal constraints and terminal weights. The proposed methods greatly reduce—and in many cases completely avoid—deadlocks. Moreover, in the case of a five-level topology, a significant reduction of the switching frequency and the harmonic distortion is observable.**

***Index Terms*—Model predictive direct torque control, model predictive control, medium-voltage drives**

I. Introduction

The increasing computational power available today facilitates the application of model predictive control (MPC) [1] to power electronic systems [2], [3], where the sampling intervals are typically below 100μs. Two different ways of using MPC for power electronics can be observed. In a first approach, the current control loop of field oriented control [4] is replaced by MPC while keeping the modulator [5]. In a second approach, also the task of the modulator is accomplished by the MPC algorithm, which manipulates the inverter switch positions directly and refrains from using a modulation scheme. This approach leads to the concept of predictive current control, see e.g. [6] and [7], and model predictive direct torque control (MPDTC) [2], [8], [9]. MPDTC can be considered as an advancement of direct torque control (DTC) [10], in which the look-up table is replaced by an online optimization stage. Specifically, the electromagnetic torque, stator flux magnitude and inverter states are kept within their respective bounds, while the switching frequency of the inverter is minimized.

Besides MPDTC's significant performance improvements regarding the switching frequency, switching losses and harmonic distortion when compared to classic DTC [9], the MPDTC algorithm tends to run occasionally into infeasible states, so called *deadlocks* [11]. These deadlocks occur for combinations of stator and rotor flux vectors, inverter states and hysteresis bounds, for which no sequence of inverter switch positions exists that keeps the controlled variables within their respective bounds.

In case of a deadlock, one option is to relax the hysteresis bounds and to minimize the predicted violation of the hysteresis bounds rather than the switching frequency [11]. This so called *infeasibility exit strategy* is executed until the deadlock has been resolved. However, the execution of this exit strategy often leads to a spike in the instantaneous switching frequency, to which we refer as a *switching burst*. In the worst case, such switching bursts could lead to a trip of the drive.

This paper proposes new methods that aim at avoiding deadlocks and thus the triggering of the infeasibility exit strategy. The proposed methods are based on the notion of terminal weights and terminal constraints [1]. As a result, the occurrence of deadlocks is drastically reduced and in many cases avoided altogether, as demonstrated for a three-level neutral point clamped (NPC) inverter. In addition to that, for a five-level topology [12], significant reductions of the switching frequency as well as of the harmonic distortions of the torque and stator currents are also achieved.

This paper is organized as follows. Sect. II summarizes the concept of MPDTC. In Sect. III the occurrence of deadlocks is analyzed in detail, whereas new deadlock avoidance strategies are proposed in Sect. IV. Sects. V and VI provide performance results of the introduced deadlock avoidance strategies for three- and five-level topologies, respectively. Conclusions are drawn in Sect. VII.

II. Model Predictive Direct Torque Control

MPDTC was proposed in [2], presented in detail in [8] and [11], and generalized in [9]. Branch and bounds methods were add in [13] to reduce the computational burden by about an order of magnitude. At steady-state operation, MPDTC

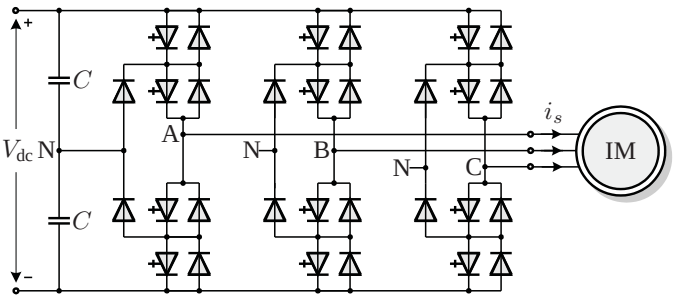

Fig. 1: NPC inverter driving an induction machine (IM)

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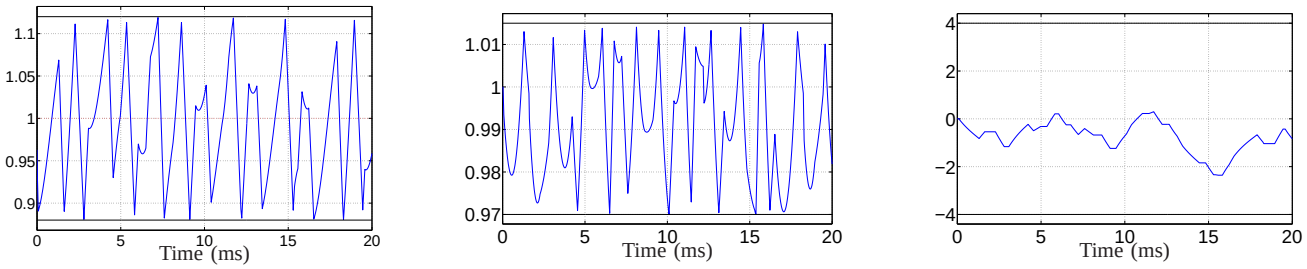


(a) Electromagnetic torque (pu) (b) Stator flux magnitude (pu) (c) Neutral point potential (%)

Fig. 2: Steady-state operation at nominal speed and torque of MPDTC for a NPC inverter with a medium-voltage induction machine. The switching horizon is 'SSE' and the switching frequency is minimized.

provides switching losses and current distortions similar to the ones typically achieved by optimized pulse patterns [14], while during transients, its dynamic response is as fast as the one of DTC [15].

This section provides a brief summary of the MPDTC approach based on the aforementioned literature and the notation used therein. The drive system initially used as a case study is assumed to consist of a three-level NPC inverter [16] with a medium-voltage squirrel-cage induction machine. The neutral point (NP) potential of the inverter floats. Fig. 1 shows the topology of the inverter. The parameters of the drive system are summarized in Table I.

A. Prediction Model

The prediction model is formulated in the stationary orthogonal $\alpha\beta$ coordinate system. The model's state vector is defined as $\boldsymbol{x} = [\psi_{s\alpha}\ \psi_{s\beta}\ \psi_{r\alpha}\ \psi_{r\beta}\ v_n]^T$, with $\psi_{s\alpha}$ and $\psi_{s\beta}$ denoting the α and β-components of the stator flux linkage, while $\psi_{r\alpha}$ and $\psi_{r\beta}$ refer to the components of the rotor flux. The potential of the NP is given by v_n.

The three-phase switch positions u_a, u_b, u_c constitute the input vector $\boldsymbol{u} = [u_a\ u_b\ u_c]^T \in \{-1, 0, 1\}^3$. The electromagnetic torque T_e, the stator flux magnitude $\Psi_s = \sqrt{\psi_{s\alpha}^2 + \psi_{s\beta}^2}$ and the NP potential v_n form the output vector $\boldsymbol{y} = [T_e\ \Psi_s\ v_n]^T$.

Combining the standard dynamical motor model of an induction machine with the model of the NP potential, as presented in Sect. II of [8], and using the forward Euler approximation approach, a discrete-time drive model in state-space form can be derived, which is of the form

$$\boldsymbol{x}(k+1) = \boldsymbol{A}\boldsymbol{x}(k) + \boldsymbol{B}\boldsymbol{u}(k) \tag{1}$$

$$\boldsymbol{y}(k) = \boldsymbol{g}(\boldsymbol{x}(k)) \tag{2}$$

and uses the sampling interval $T_s = 25\mu$s. The definition of the matrices $\boldsymbol{A}$ and $\boldsymbol{B}$ and vector $\boldsymbol{g}$ can be found in the appendix of [8].

Induction machine	Voltage	3300 V	R_s	0.0108 pu
	Current	356 A	R_r	0.0091 pu
	Real power	1.587 MW	L_{ls}	0.1493 pu
	Apparent power	2.035 MVA	L_{lr}	0.1104 pu
	Frequency	50 Hz	L_m	2.3489 pu
	Rotational speed	596 rpm		
Inverter			V_{dc}	1.930 pu
			C	11.769 pu

TABLE I: Rated values (left) and parameters (right) of the NPC inverter drive system

B. Optimization Problem

The control problem is to keep the machine's torque and stator flux magnitude as well as the inverter's NP potential within given (hysteresis) bounds around their respective references. The switching losses in the semiconductors are to be minimized. An indirect way of achieving this is to minimize the device switching frequency[1].

Writing the above control problem as a closed-form optimization problem leads to

$$J^*(\boldsymbol{x}(k),\boldsymbol{u}(k-1)) = \min_{\boldsymbol{U}(k)} \left(J_{\text{sw}} + J_t\right) \tag{3a}$$

$$\text{s.t. } \boldsymbol{x}(\ell+1) = \boldsymbol{A}\boldsymbol{x}(\ell) + \boldsymbol{B}\boldsymbol{u}(\ell) \tag{3b}$$

$$\boldsymbol{y}(\ell+1) = \boldsymbol{g}(\boldsymbol{x}(\ell+1)) \tag{3c}$$

$$\boldsymbol{y}(\ell+1) \in \boldsymbol{\mathcal{Y}} \tag{3d}$$

$$\boldsymbol{u}(\ell) \in \boldsymbol{\mathcal{U}}\,, \quad ||\Delta\boldsymbol{u}(\ell)||_\infty \leq 1 \tag{3e}$$

$$\forall \ell = k, \ldots, k+N_p-1\,, \tag{3f}$$

with J^* denoting the minimum of the objective function $J = J_{\text{sw}} + J_t$. The first term of J captures the instantaneous switching frequency

$$J_{\text{sw}} = \frac{1}{N_p} \sum_{l=k}^{k+N_p-1} \|\Delta\boldsymbol{u}(\ell)\|_1 \tag{4}$$

with $\Delta\boldsymbol{u}(\ell) = \boldsymbol{u}(\ell) - \boldsymbol{u}(\ell-1)$. The second term J_t is an optional term that will be introduced in Sect. IV.

The lower and upper bounds on the controlled variables form the set $\boldsymbol{\mathcal{Y}} = [\underline{T}_e, \overline{T}_e] \times [\underline{\Psi}_s, \overline{\Psi}_s] \times [\underline{v}_n, \overline{v}_n]$, where $\underline{T}_e$ ($\overline{T}_e$) refers to the lower (upper) torque bounds. The bounds on the stator flux magnitude and NP potential are defined accordingly.

The constraint (3e) limits the control input $\boldsymbol{u}$ to the integer values $\boldsymbol{\mathcal{U}} = \{-1, 0, 1\}^3$ available for the three-level inverter.

[1]Alternatively, the switching losses can be directly targeted [9].

Switching in a phase by more than one step up or down is not allowed to avoid a shoot-through. This restriction is enforced by the second constraint in (3e), $||\Delta \boldsymbol{u}(\ell)||_\infty \leq 1$, which limits the elements in $\Delta \boldsymbol{u}$ to ± 1. These constraints have to be met at every time-step ℓ within the prediction horizon. The sequence of control inputs $\boldsymbol{U}(k) = [\boldsymbol{u}(k), \ldots, \boldsymbol{u}(k + N_p - 1)]$ over the prediction horizon N_p represents the sequence of inverter switch positions the controller decides upon. The objective function (3a) is to be minimized for all $\boldsymbol{U}(k)$ subject to the dynamical evolution of the drive (3b), its outputs (3c) and the constraints (3d) and (3e).

C. MPDTC Algorithm

An important part of the MPDTC algorithm is the so called switching horizon, which consists of a certain chronological order of switching events 'S' and extrapolation steps 'E'. In the case of the switching horizon 'SSE', for example, the algorithm has the freedom to switch the input vector $\boldsymbol{u}$ at time-steps k and $k+1$ ('SS') with respect to (3e). Thereafter, the second input vector $\boldsymbol{u}(k+1)$ is locked in and the controlled variables $\boldsymbol{y}$ are extrapolated ('E') for as long as the constraints (3d) are satisfied. The time-instant (3d) is violated defines the length of the prediction horizon N_p. As a result, N_p is not of fixed length as it is common for MPC, but varies with the switching sequences. Based on the switching horizon and the constraints defined in (3), the MPDTC algorithm establishes all feasible switching sequences $\boldsymbol{U}(k)$ together with their corresponding costs J and selects the sequence with the minimal cost.

A detailed description of the generalized MPDTC algorithm can be found in Sect. III of [9]. Fig. 2 shows an example of the waveforms of the three output variables over 20 ms at steady state operation and rated speed and torque, when using the switching horizon 'SSE'. Throughout the paper, if not otherwise stated, 'SSE' will be used.

III. Occurrence of Deadlocks

A. Definition of Deadlocks

An infeasible state is a state vector $\boldsymbol{x}(k)$ for which the set of candidate switching sequences is empty at Step 3 of the MPDTC algorithm, as defined in [8]. This implies that there exists no switching sequence that is predicted to keep the output variables within their bounds over the prediction horizon, assuming that the output variables are within their respective bounds at time-step k. Correspondingly, if output variables are outside of their bounds, there exists no candidate switching sequence that reduces the bound violation at every time-step within the prediction horizon. A deadlock is the situation in which an infeasible state arises. This implies that the control problem (3) is infeasible and cannot be solved.

B. Root Cause Analysis of Deadlocks

Deadlocks are caused by the combination of the output variables being constrained between upper and lower bounds and the fact that the switch positions are restricted to a finite and discrete-valued set. In order to characterize these deadlocks, the mathematical analysis provided in [2] and [11] is summarized hereafter. Based on the standard state-space equations of an induction machine and the expression for the electromagnetic torque, the following approximate equations can be derived.

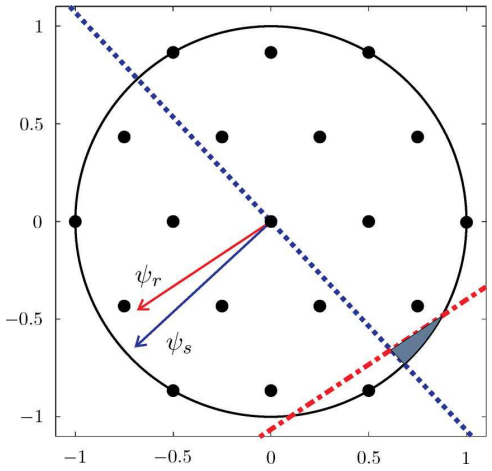


Fig. 3: Root cause of deadlocks. The set of discrete voltage vectors in the $\alpha\beta$-plane is enclosed by a circle, which contains all relaxed voltage vectors. The circle, together with the constant torque (red dash-dotted) line and the constant stator flux magnitude (blue dotted) line define the hatched feasible region. This region contains the relaxed voltage vectors that achieve the desired control command (increase torque, reduce stator flux magnitude). Since in this example, the feasible region contains no discrete-valued voltage vectors, the control problem is infeasible. This figure has been taken from [11].

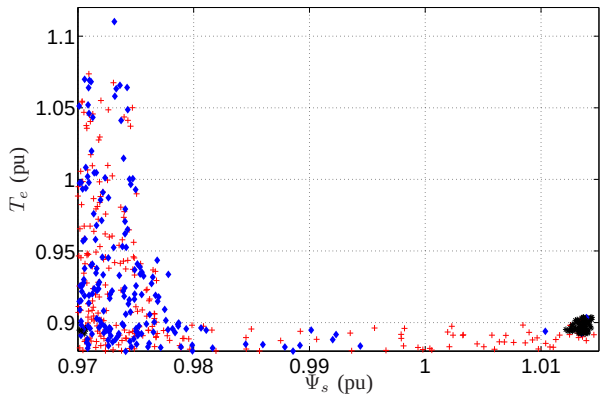
$$\frac{dT_e}{dt} = 0 \Longleftrightarrow |\boldsymbol{\psi}_r \times \boldsymbol{v}| = \left(\boldsymbol{\psi}_s^T \boldsymbol{\psi}_r\right) \omega \tag{5}$$

$$\frac{d\boldsymbol{\psi}_s}{dt} = 0 \Longleftrightarrow \boldsymbol{\psi}_s^T \boldsymbol{v} = 0\,, \tag{6}$$

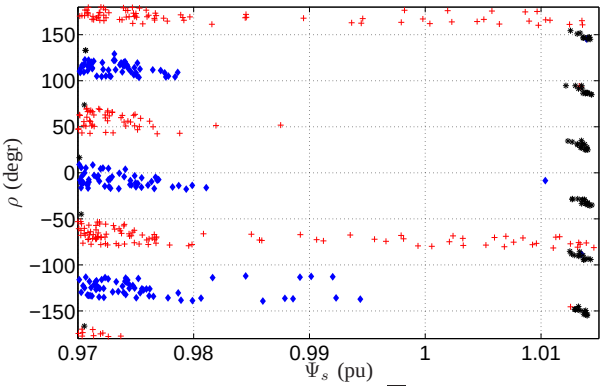
where $\boldsymbol{\psi}_s = [\psi_{s\alpha}\ \psi_{s\beta}]^T$ is the stator flux vector, $\boldsymbol{\psi}_r = [\psi_{r\alpha}\ \psi_{r\beta}]^T$ the rotor flux vector, ω the rotor's rotational speed and $\boldsymbol{v}_{\alpha\beta} = [v_\alpha\ v_\beta]^T$ denotes the voltage vector. The latter is obtained by the transformation of the three-phase voltages $\boldsymbol{v}_{abc} = [v_a\ v_b\ v_c]^T$ to the orthogonal $\alpha\beta$ coordinate system.

For a symmetrical and sinusoidal three-phase system with constant amplitude and frequency, the voltage vector that achieves constant flux and torque rotates with the same frequency and a constant amplitude around the origin of the complex $\alpha\beta$ plane. We refer to this continuous-valued vector as the *relaxed* voltage vector. For a converter system, however, only a finite number of discrete-valued voltage vectors is available. These are shown as black dots in Fig. 3, assuming a three-level inverter.

Considering the α and β-components of the relaxed voltage vector as free variables, (5) describes a line in the $\alpha\beta$-plane that is parallel to the rotor flux vector. This line is referred to as the constant *torque* line. Voltage vectors that lie between this line and the origin decrease the torque, voltage vectors beyond this line increase it. Note that increasing the speed (and therefore the modulation index) shifts the constant torque line away from the origin and reduces the number of discrete-valued voltage vectors. The control problem thus becomes harder to solve.



(a) Deadlocks as a function of $\Psi_s \in [\underline{\Psi}_s,\ \overline{\Psi}_s]$ and $T_e \in [\underline{T}_e,\ \overline{T}_e]$.



(b) Deadlocks as a function of $\Psi_s \in [\underline{\Psi}_s,\ \overline{\Psi}_s]$ and $\rho \in [-180°,\ 180°]$, where ρ is the angle between the rotor flux vector and the α-axis of the $\alpha\beta$ reference frame.

Fig. 4: Deadlocks at nominal speed and torque. Depending on their type, the deadlocks form clearly visible and distinguishable clusters.

Eqn. (6) describes a line in the $\alpha\beta$-plane that is perpendicular to the stator flux vector and intersects the origin. This line is referred to as the constant *stator flux magnitude* line. Voltage vectors that lie on the same side of this line as the stator flux vector increase the stator flux magnitude, voltage vectors that lie on the opposite side decrease it. Fig. 3 shows an example of a typical deadlock situation based on the foregoing, theoretical considerations.

The previous analysis focused on the torque and stator flux magnitude. When the NP potential is taken into account as well, a further restriction on the voltage vector is added. Each switch position that corresponds to at least one phase connected to the NP, has a particular influence on it, depending on the sign of the phase current. Even if a voltage vector is available that satisfies the required control commands for the torque and the stator flux magnitude, the corresponding switch position might lead to a violation of the NP potential's bounds.

C. Location of Deadlocks in the State-Space

As will be shown in this section, in case of the NPC inverter, deadlocks tend to occur in the following two cases.

- The electromagnetic torque is close to its lower bound and needs to be increased, while the stator flux magnitude is at its upper bound and is to be reduced, regardless of the value of the NP potential. We refer to these deadlocks as *Type M* deadlocks, with *M* referring to the fact that only the two output variables of the machine give rise to the deadlock.
- The torque or the stator flux magnitude are at their lower bound and need to be increased, while the NP potential is close to one of its bounds. We refer to this as *Type N* deadlocks, where N refers to the fact that the NP, too, is involved.

To determine the location of infeasible states in the state-space, a simulation was run at nominal speed and torque over 1000 fundamental periods, as shown in Fig. 4. Depending on the value of the NP potential, the deadlocks are divided into the following three groups, and individual colors and markers are assigned to each group.

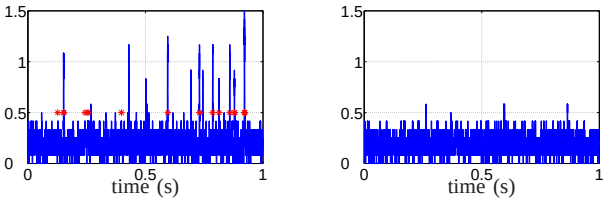
$$\begin{aligned}
&\text{red (+)}, && \text{if } v_n \geq \overline{v}_n - \Delta v_n \text{ (\textit{Type N})}\\
&\text{black (*)}, && \text{if } v_n \in [\underline{v}_n + \Delta v_n, \overline{v}_n - \Delta v_n] \text{ (\textit{Type M})}\\
&\text{blue ($\diamond$)}, && \text{if } v_n \leq \underline{v}_n + \Delta v_n \text{ (\textit{Type N})},
\end{aligned}$$

where $\Delta v_n = 0.006(\overline{v}_n - \underline{v}_n)$. The first and third group (*Type N*) correspond to deadlocks, in which the NP potential is close to or violates its upper or lower bound, respectively. The second group (*Type M*) refers to deadlocks, in which the NP potential is clearly within its bounds.

Fig. 4(a) depicts all deadlocks as a function of $T_e \in [\underline{T}_e,\ \overline{T}_e]$ and $\Psi_s \in [\underline{\Psi}_s,\ \overline{\Psi}_s]$, i.e. the torque and flux magnitude values within its bounds. The drive is operated at nominal speed, torque and flux. *Type M* deadlocks are concentrated in the lower right corner. In this region, a voltage vector is required that increases the torque and decreases the flux magnitude. This corresponds exactly to the situation discussed in the foregoing analysis in Sect. III-B, which is visualized in Fig. 3.

Type N deadlocks also reveal a certain pattern, namely they occur close to the lower bounds of the torque and flux magnitude, particularly in the lower left corner, where both conditions are met. The reason why they occur exactly in this way is hard to describe in a formal way since the neutral point is involved as well. The plot indicates that *Type M* and *Type N* deadlocks exhibit a distinctive behavior and suggests that they ought to be handled separately, as will be discussed in more detail in Sect. IV.

Fig. 4(b) depicts all deadlocks as a function of $\Psi_s \in [\underline{\Psi}_s,\ \overline{\Psi}_s]$ and $\rho \in [-180°, 180°]$ for all $T_e \in [\underline{T}_e,\ \overline{T}_e]$, where ρ is the angle between the rotor flux vector and the α-axis of the $\alpha\beta$ reference frame. The *Type M* deadlocks appear in intervals of $60°$ due to the $60°$-symmetry of the voltage vectors. The *Type N* deadlocks appear in intervals of $120°$ due to the significant third-harmonic component of the NP potential [17]. Note that the general deadlock pattern of Fig. 4 for nominal speed is representative for all other velocities, too.



(a) Original MPDTC version (b) MPDTC with Approach A_1B

Fig. 5: Evolution of the instantaneous switching frequency (kHz) at nominal speed and torque for the NPC inverter over 1 s. The red stars in Fig. 5(a) indicate the occurrence of deadlocks. A strong correlation between deadlocks and switching bursts can be observed.

D. Deadlock Resolution Strategy

In the context of MPC, infeasibility problems are usually resolved by relaxing some of the control problem's constraints [18]. In the case of MPDTC, the main constraint leading to deadlocks is the restriction of the inverter switch positions to be discrete-valued, rather than real-valued; this constraint cannot be relaxed. Instead, the hysteresis bounds are relaxed, by modifying the optimality criterion. Specifically, instead of minimizing the switching frequency, the predicted violation of the hysteresis bounds at time-step $k+1$ is computed and the voltage vector that minimizes this violation is chosen [11]. This so called *infeasibility exit strategy* is executed once the control algorithm has encountered a deadlock, and it is applied until the deadlock has been resolved.

E. Switching Bursts

This infeasibility exit strategy reliably resolves all deadlocks and ensures the stability of the system. It often requires, however, several switching transitions within a short time-interval, leading to a spike in the instantaneous switching frequency, to which we refer as a *switching burst*. For the safe operation of the inverter, it is mandatory for the instantaneous switching frequency to be constant. Spikes can lead to local overheating and might prevent the gate drivers from fully recharging. In the worst case, switching bursts can lead to the tripping of the drive system.

We define the *instantaneous* switching frequency as the average number of switching events (of all switching devices) during the last 1 ms. The instantaneous switching frequency is updated at every sampling step. Fig. 5(a) shows the instantaneous switching frequency of MPDTC. Characteristic peaks can be observed, which clearly correlate with the occurrence of deadlocks, denoted by red stars. This indicates that deadlocks cause switching bursts; avoiding deadlocks avoids these bursts, as can be seen in Fig. 5(b).

IV. Deadlock Avoidance Strategies

In the following, three different families of deadlock avoidance strategies (Approaches A, B and C) are presented. These are based on terminal soft constraints, terminal weights and exact deadlock prediction, respectively. While Approaches A and C can be applied both to *Type M* and *Type N* deadlocks, Approach B, which uses a terminal weight, is restricted to *Type N* deadlocks.

A. Approach A_1: Terminal Soft Constraint on Torque and Stator Flux Magnitude

The following *terminal soft constraint* is added as an additional term J_t to the cost function (3a)

$$J_t = \begin{cases} \lambda_m & \text{if } \boldsymbol{y}(k+N_p) \in \boldsymbol{\mathcal{Y}}_c \\ 0 & \text{else}\,, \end{cases} \tag{7}$$

where $\boldsymbol{\mathcal{Y}}_c$ represents the so called critical region for the electromagnetic torque and stator flux magnitude

$$\boldsymbol{\mathcal{Y}}_c = \{\boldsymbol{y} \,|\, T_e \leq \underline{T}_e + \Delta T_e\} \cap \{\boldsymbol{y} \,|\, \Psi_s \geq \overline{\Psi}_s - \Delta\Psi_s\} \cap \boldsymbol{\mathcal{Y}}\,. \tag{8}$$

The set $\boldsymbol{\mathcal{Y}}_c$, comprising the bottom right corner in Fig. 4(a), correlates with a high likelihood of *Type M* deadlocks. The variables ΔT_e and $\Delta\Psi_s$ are chosen such that all *Type M* deadlocks are covered, whilst $\boldsymbol{\mathcal{Y}}_c$ is as small as possible. The weight λ_m is very large.

The terminal soft constraint (7) has the following effect on the selection process of the optimal switching sequence. If there is at least one sequence such that $J_t = 0$ holds, implying that its output trajectory does not terminate in the critical region, then only switching sequences are considered such that the constraint

$$\boldsymbol{y}\,(k+N_p) \in \boldsymbol{\mathcal{Y}} \setminus \boldsymbol{\mathcal{Y}}_c\,, \tag{9}$$

is met. Out of this set of switching sequences, the one with the lowest cost (switching frequency) J_{sw}, which is the original cost function, is chosen as the optimal sequence. All switching sequences with $J_t = \lambda_m$ are suboptimal.

If no sequence with $J_t = 0$ exists, i.e. all sequences drive the outputs into the critical region, then (9) is implicitly relaxed and all sequences are considered. Therefore, (7) is equivalent to the constraint (9), which is soft, i.e. can be relaxed. The proposed method only performs well, if the critical region is well defined and small compared with $\boldsymbol{\mathcal{Y}}$, since MPDTC loses a certain degree of freedom, potentially impacting the performance. In our case, these two conditions are satisfied.

B. Approach A_2: Terminal Soft Constraint on Torque, Stator Flux Magnitude and NP Potential

The terminal soft constraint can be extended to also address the NP and therefore *Type N* deadlocks. The critical region is then defined as $\boldsymbol{\mathcal{Y}}_c' = \boldsymbol{\mathcal{Y}}_c \cap \boldsymbol{\mathcal{Y}}_n$ with

$$\boldsymbol{\mathcal{Y}}_n = \{\boldsymbol{y} \,|\, v_n \leq \underline{v}_n + \Delta v_n\} \cup \{\boldsymbol{y} \,|\, v_n \geq \overline{v}_n - \Delta v_n\}\,, \tag{10}$$

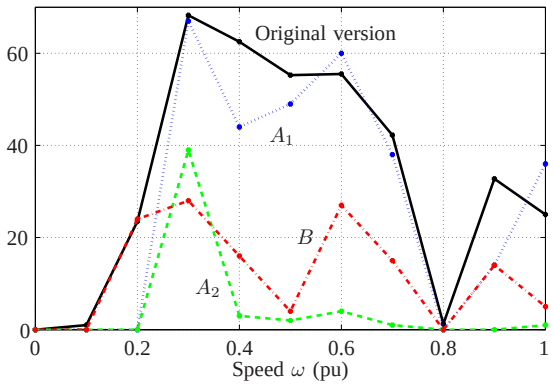
where Δv_n was defined in Section III-C.

C. Approach B: Terminal Weight on NP Potential

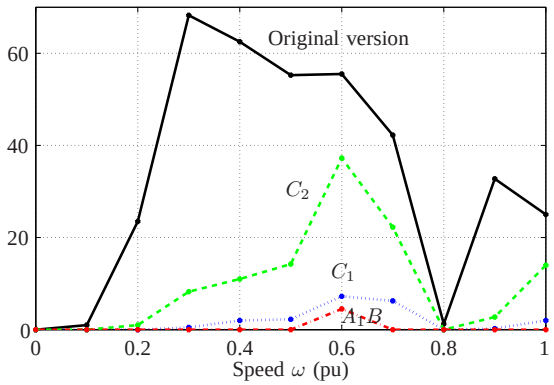
Approach B focuses on the NP trajectory and thus on *Type N* deadlocks. The quadratic terminal weight

$$J_t = \lambda_n \big(v_n(k+N_p)\big)^2 \tag{11}$$

is added to the cost function (3a), where λ_n is a tuning parameter. As a result, NP trajectories ending close to the reference, which is typically zero, are penalized little, whereas trajectories with significant deviations are penalized severely.



(a) Approaches A_1, A_2 and B compared with the original MPDTC version



(b) Approaches A_1B, C_1 and C_2 compared with the original MPDTC version

Fig. 6: Frequency of deadlocks (Hz) as function of the speed ω. The results of the original MPDTC version and the Approaches A_1, A_2, B, A_1B, C_1 and C_2 are depicted.

D. Approach A_1B: Combination of Approaches A_1 and B

The terminal soft constraint on the torque and stator flux trajectories (Approach A_1) can be combined with the terminal weight on the NP trajectory (Approach B), by adding both (7) and (11) to the cost function (3a).

E. Approach C_1: Deadlock Prediction at Time-Step $k+N_p$

Approach C adds a post-processing step to the MPDTC algorithm. Once the switching sequences have been enumerated and a potentially optimal switching sequence $\boldsymbol{U}^*(k)$ has been determined, a deadlock prediction step is executed according to the following procedure:

1) Given $\boldsymbol{U}^*(k)$, the terminal state $\boldsymbol{x}^*(k+N_p)$ is calculated using (3b).
2) Using $\boldsymbol{x}^*(k+N_p)$ as new initial state, the existence of at least one switching sequence $\boldsymbol{U}(k+N_p)$ starting at $k+N_p$ is evaluated that meets the constraints (3b)–(3e) at the time-steps $k+N_p+1,\ldots,k+N_p+N_s$. Note that N_s equals the minimum length of a feasible switching sequence.

3a) If such a $\boldsymbol{U}(k+N_p)$ exists, this serves as a proof that under nominal conditions (no model mismatches, no reference changes, no measurement errors) the optimal switching sequence $\boldsymbol{U}^*(k)$ does *not* lead into a deadlock.

3b) If no feasible $\boldsymbol{U}(k+N_p)$ is found in step 2), $\boldsymbol{U}^*(k)$ is discarded, the second best sequence is chosen as optimal sequence $\boldsymbol{U}^*(k)$ and the procedure is repeated, starting at step 1).

In this iterative way, all candidate switching sequences, starting with the one with the lowest cost, are analyzed in ascending order of their cost, until one is found that does not lead into a deadlock. If no such sequence exists, the one with the lowest cost is selected, similar to Approach A_1.

F. Approach C_2: Deadlock Prediction at Time-Step $k+1$

A modified version of Approach C uses $\boldsymbol{x}^*(k+1)$ as the new initial state, rather than $\boldsymbol{x}^*(k+N_p)$. Looking only one instead of N_p steps ahead, adds robustness to the strategy, since $\boldsymbol{x}^*(k+1)$ can be predicted more accurately than $\boldsymbol{x}^*(k+N_p)$, particularly when the prediction horizon is very long.

V. Performance Results for the NPC Inverter

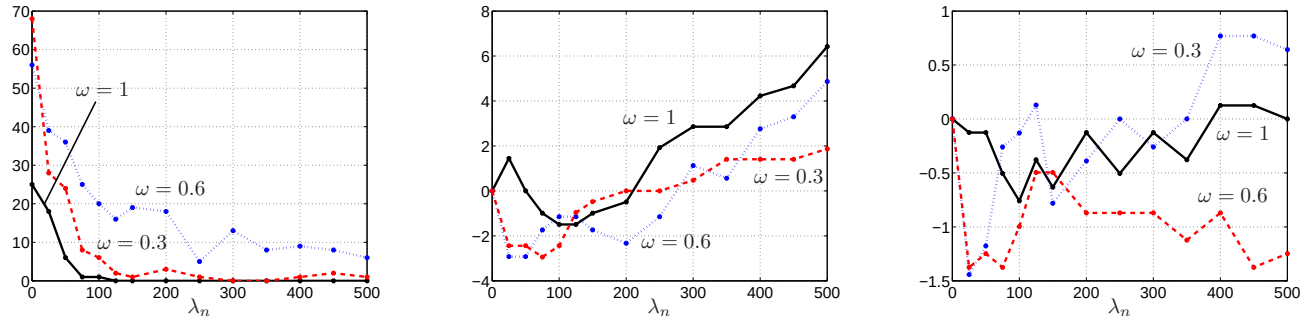
Performance results of the proposed deadlock avoidance strategies are presented hereafter. Their influence on the frequency of deadlocks, the occurrence of switching bursts and the performance are investigated. The NPC inverter driving a medium-voltage induction machine shown in Fig. 1 is used, with its parameters given in Table 1 in [7].

A. Effect on the Frequency of Deadlocks

At nominal torque, Fig. 6 depicts the number of deadlocks as a function of the speed ω for all proposed deadlock avoidance approaches. In both figures, the straight (black) lines refer to the original MPDTC version, serving as a benchmark. Fig. 6(a) presents the results for Approaches A_1, A_2 and B, whereas Fig. 6(b) focuses on Approaches A_1B, C_1 and C_2. Approach A_1B avoids all deadlocks except for at $\omega = 0.6$. Considering the results of A_1 and B separately, one can see that the effect of Approach A_1B is not simply the sum of A_1 and B, but rather the synergy of both. A detailed analysis showed that Approach A_1 significantly reduces *Type M* deadlocks, while increasing *Type N* deadlocks, with the overall result not showing a significant improvement. If A_1 is however combined with Approach B, which reliably resolves all *Type N* deadlocks, this negative effect is compensated for, resulting in a very good overall performance. Approaches A_2 and C_1 work nearly as well as A_1B in terms of deadlock reduction, while C_2 is less successful.

B. Effect on Switching Bursts

As previously mentioned, the observed correlation between deadlocks and switching bursts leads to the assumption that with the avoidance of deadlocks also the switching bursts can be avoided. Fig. 5(a) shows the instantaneous switching



(a) f_{DL} (Hz) (b) Δf_{sw} (%) (c) ΔI_{THD} (%)

Fig. 7: Approach $\mathrm{A}_1\mathrm{B}$: Frequency of deadlocks f_{DL}, deviation in switching frequency Δf_{sw} and deviation in current THD ΔI_{THD} as a function of the terminal weight λ_n on the NP potential for three different velocities $\omega \in \{0.3, 0.6, 1\}$.

frequency for the original MPDTC version, with clearly identifiable switching bursts. Approach $\mathrm{A}_1\mathrm{B}$ successfully avoids all switching bursts, as shown in Fig. 5(b).

This is not achieved by the other promising approaches, i.e. A_2, C_1 and C_2. It appears that for these approaches the effort in terms of switching events to avoid deadlocks is similar to the effort to resolve deadlocks using the infeasibility exit strategy. In other words, for Approaches A_2, C_1 and C_2, the switching bursts are only shifted, not removed.

Additional investigations revealed that *Type N* deadlocks are the dominant cause of switching bursts, and that these deadlocks are in general more difficult to resolve than deadlocks caused by the torque or flux (*Type M* deadlocks). It is therefore paramount to efficiently avoid *Type N* deadlocks. Only Approach B, based on a terminal weight on the NP potential, works in an excellent way, avoiding *Type N* deadlocks and switching bursts. The terminal weight reduces the fluctuation of the NP potential around its reference gently and smoothly.

C. Effect of the Approach A_1B on the Performance

Since only Approach $\mathrm{A}_1\mathrm{B}$ avoids deadlocks as well as switching bursts, the further investigation is restricted to it. In the following, the effect of $\mathrm{A}_1\mathrm{B}$ on the switching frequency f_{sw}, the total harmonic distortions (THD) of the current and torque, I_{THD} and T_{THD}, respectively, and the frequency of deadlocks f_{DL} are investigated and discussed. Using the original MPDTC version as a baseline, these performance values are normalized and their percentagewise deviation from the original version is shown, e.g. $\Delta f_{sw} = (f_{\mathrm{sw}}^{\mathrm{A_1B}} - f_{\mathrm{sw}}^{\mathrm{org}})/f_{\mathrm{sw}}^{\mathrm{org}}$.

ω (pu)	Δf_{sw} (%)	ΔI_{THD} (%)	ΔT_{THD} (%)	f_{DL} (Hz)	λ_n
1	-2	-0.9	-0.6	0	125
0.9	-1.3	-0.25	-0.2	0	75
0.8	0	0	0	0	0
0.7	0	-0.6	0.2	0	50
0.6	-1.13	-0.4	-1.6	4.5	250
0.5	-2.5	-1	0.3	0	125
0.4	-0.9	-2	0.8	0	150
0.3	0.5	-0.9	1.4	0	300
0.2	0	-1.2	-0.3	0	75
0.1	0	-0.5	0	0	25

TABLE II: Performance improvement in percent resulting from Approach $\mathrm{A}_1\mathrm{B}$, using the original MPDTC version as a baseline.

Fig. 7 shows f_{DL}, Δf_{sw} and ΔI_{THD} as a function of the terminal weight λ_n imposed on the NP potential. Three different velocities $\omega \in \{0.3, 0.6, 1\}$ are investigated. As λ_n is increased, the NP potential is kept more tightly around its reference and the number of deadlocks is reduced accordingly, which tends to also reduce the switching frequency. Large λ_n, however, entail a higher control effort, resulting in an increase in the switching frequency.

The influence of λ_n on the current distortion is small, since it depends primarily on the hysteresis bounds on the stator flux. Nevertheless, less fluctuations of the NP potential provide less "distorted" voltage vectors, and avoiding deadlocks prevents potential bound violations. Both aspects have a positive impact on the current THD, as it is visible in Fig. 7(c).

Fig. 7 also reveals that the benefit of the terminal weight is similar for all speeds. To obtain excellent results, however, λ_n has to be tuned speed-dependent, as summarized in Table II.

VI. Performance Results for the ANPC Inverter

A. Control Scheme for the 5L ANPC Inverter

This section considers a medium-voltage drive system comprising a 6.6 kV induction machine and the five-level active neutral point clamped (ANPC) inverter shown in Fig. 8, which was recently proposed in [12] and introduced as a commercial product in [19]. Featuring in each phase a flying capacitor charged to one forth of the dc-link voltage, five voltage levels per phase can be synthesized. The parameters of the five-level ANPC drive system considered in this section are provided in Table III.

Current control and modulation is achieved by a hierarchical control scheme. The upper layer is based on offline computed optimal pulse patterns (OPPs), which minimize the current THD for a given switching frequency [14]. Fast closed-loop control of the machine currents is achieved by controlling the stator flux vector along its reference trajectory, manipulating the switching instants of the OPPs online, using the principle of model predictive control. We refer to this control scheme

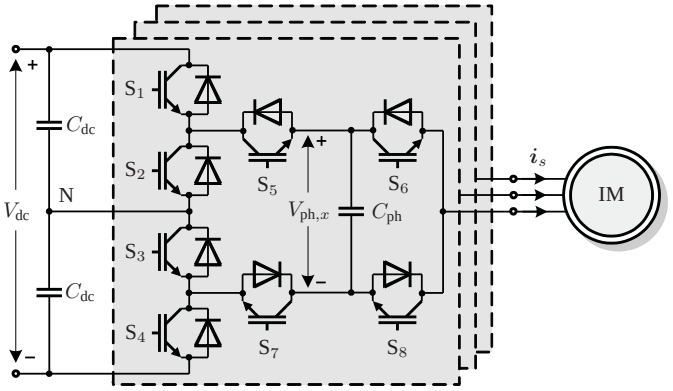


Fig. 8: Equivalent representation of the five-level active neutral point clamped (ANPC) voltage source inverter driving an induction machine (IM)

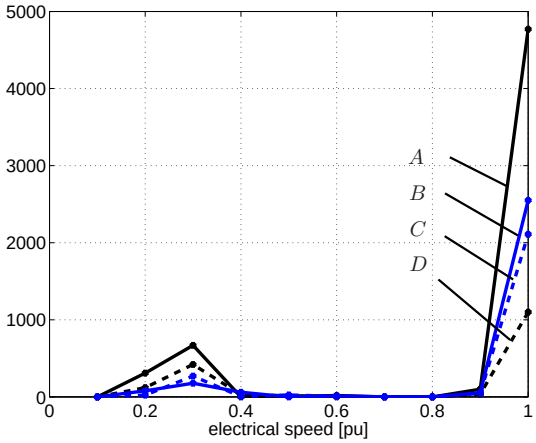


Fig. 9: Number of deadlocks per second as function of the electrical speed. The two switching horizons 'SSE' and 'SESE' were investigated, each of them for the pulse numbers $d = 6$ and $d = 10$. The four resulting combinations are A: 'SESE' and $d = 6$; B: 'SSE' and $d = 6$; C: 'SSE' and $d = 10$; and D: 'SESE' and $d = 10$.

as model predictive pulse pattern control (MP^{3}C), which is described in detail in [20] and applied to the ANPC topology in [21].

The lower control layer keeps the NP potential and the phase capacitor voltages within bounds around their references, exploiting the three-phase redundancy of the voltage vectors and the single-phase redundancy of the phase states. We refer to this control scheme as model predictive direct balancing control (MPDBC) [22], which is a derivative of MPDTC. Analogous to MPDTC, the predictive balancing algorithm uses a switching horizon, extrapolation and bounds, within which the output variables are kept, while minimizing the switching frequency.

In summary, MP^{3}C controls the machine and derives an optimal sequence of voltage vectors, based on which MPDBC controls the internal inverter voltages (NP potential and three phase capacitor voltages), providing the firing signals for the semiconductors. As a result, the issue of deadlocks is restricted to MPDBC. An analysis over the whole speed range reveals that many deadlocks occur at nominal speed $\omega = 1$ and a few around $\omega = 0.3$, see Fig. 9. In the following, two deadlock avoidance schemes are proposed, one for nominal and one for low speed.

B. Deadlock Avoidance at Nominal Speed

When neglecting the NP potential, it is a characteristic of the ANPC inverter that a redundant switch position always exists that reverses the current through the phase capacitors, thus enabling the balancing of their voltages. When also considering the NP potential, this statement does no longer hold. At nominal speed, outer voltage vectors are predominantly used, which exhibit very little redundancy, restricting the degrees of freedom of MPDBC. This tends to lead to a significant number of deadlocks, in which the NP potential and one (or more) phase capacitor voltages act as antagonists.

Since MPDBC is a derivative and tailored form of MPDTC, the same deadlock avoidance methods as introduced in Sect. IV can be used. For the deadlocks at nominal speed, Approach B, which imposes a *terminal weight* on the deviation of the NP potential from its reference, is investigated. For an appropriate value of λ_n, all deadlocks and all switching bursts can be successfully avoided, as can be seen in Fig. 10. Table IV presents the performance improvement in percent for the switching horizon 'SSE' and the pulse numbers $d = 6$ and $d = 10$, using the original MPDBC version as a baseline. As can be seen, the switching frequency can be reduced by approximately 20%, while simultaneously reducing the current and torque THDs by more than 10%. All deadlocks are removed, when using the terminal weight $\lambda_n = 1.15$ on the NP potential.

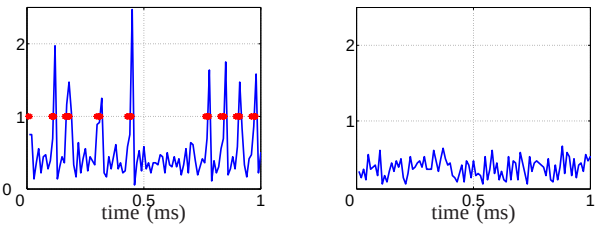
Induction motor	Voltage	6000 V	R_s	0.0057 pu
	Current	98.9 A	R_r	0.0045 pu
	Real power	850 kW	L_{ls}	0.0894 pu
	Apparent power	1.028 MVA	L_{lr}	0.0930 pu
	Frequency	50 Hz	L_m	2.492 pu
	Rotational speed	1494 rpm		
Inverter			V_{dc}	2.000 pu
			C_{dc}	2.201 pu
			C_{ph}	1.541 pu

TABLE III: Rated values (left) and per unit parameters (right) of the drive

C. Deadlock Avoidance at Low Speed

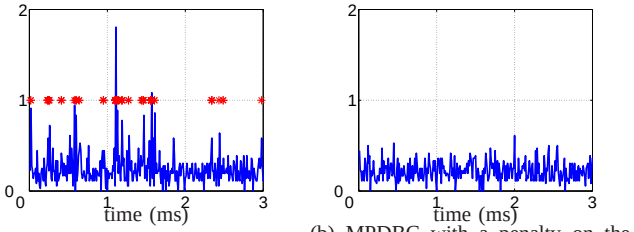
The deadlocks occurring at low speed around $\omega = 0.3$ are of a different kind and require another avoidance strategy. In this operating regime, short voltage vectors with a three-phase redundancy of four are available. Each of these redundant voltage vectors corresponds to a different common mode voltage. As an example, consider the set of voltage vectors [1 1 2], [0 0 1], [-1 -1 0] and [-2 -2 -1]. Switching between these three-phase redundant voltage vectors requires switching in all three phases, incurring a high switching cost.

Deadlocks tend to occur when using such a voltage vector with a particular large or small common mode voltage—in the example above [1 1 2] or [-2 -2 -1]. Since switching the common mode by more than one level up or down is



(a) Original MPDBC version (b) MPDBC with Approach B

Fig. 10: Evolution of the instantaneous switching frequency (kHz) at nominal speed and torque for the ANPC inverter over 1 ms. The switching horizon 'SSE' is used along with the pulse number $d = 6$. The red stars indicate the occurrence of deadlocks.



(a) Original MPDBC version (b) MPDBC with a penalty on the common mode voltage

Fig. 11: Evolution of the instantaneous switching frequency (kHz) at $\omega = 0.3$ and nominal torque for the ANPC inverter over 3 ms. The switching horizon 'SSE' is used along with the pulse number $d = 6$. The red stars indicate the occurrence of deadlocks.

prohibitively expensive and would require an extremely long prediction horizon over which to discount the commutations, MPDBC often fails to achieve this.

This excessive redundancy in the voltage vectors leads to deadlocks, which can be resolved by adding a penalty on the highest and lowest common mode levels. As is indicated in Fig. 11, this approach works well, removing all deadlocks at low speed.

VII. Conclusion

For a NPC inverter drive system, this paper shows that the deadlocks encountered during the execution of the model predictive direct torque control (MPDTC) algorithm can be separated into two groups. The first group comprises the deadlocks that are exclusively caused by the interplay between the torque and stator flux magnitude of the machine. The second group consists of deadlocks, where the NP potential is also involved, being close to one of its bounds or even violating them. Furthermore, it is highlighted that these deadlocks trigger spikes in the instantaneous switching frequency, so called switching bursts. To prevent the MPDTC algorithm from running into deadlocks, a combination of terminal *constraints* on the electromagnetic torque and stator flux magnitude together with a terminal *weight* on the NP potential is proposed. This minor modification to the original MPDTC algorithm successfully avoids all deadlocks over the whole speed range. As a result, the switching bursts are also avoided, while no significant performance loss, such as an increase in the switching frequency or the current THD, is caused by the introduced methods.

This deadlock avoidance method is also applicable to drives with more complicated inverter topologies such as the five-level ANPC inverter drive system, as briefly discussed in the previous section of this paper. Unlike for the NPC inverter, for which only the NP potential must be balanced, for the five-level topology also the three phase capacitor voltages must be controlled, greatly complicating the task of the model predictive direct balancing controller (MPDBC). The introduction of a terminal *weight* on the NP potential maintains the latter closer to its reference value and greatly reduces the balancing effort required for the NP potential. At low speed, a penalty on the common mode voltage is imposed. As a result, the deadlocks and switching bursts are not only avoided, but a significant improvement of the overall performance is also observable. At nominal speed, with respect to the baseline MPDBC method, the average switching frequency and the current THD are reduced by 20% and 13%, respectively, as detailled in [17].

The deadlock avoidance strategies proposed in this paper can be directly applied also to the other members of the MPDTC family, notably to model predictive direct current control (MPDCC) [7], which is a derivative of MPDTC, and to model predictive direct power control (MPDPC); the latter being the adaptation of MPDTC to grid-connected converters [23].

d	Δf_{sw} (%)	ΔI_{THD} (%)	ΔT_{THD} (%)	f_{DL} (Hz)	λ_n
6	-18.16	-16.11	-19.49	0	1.15
10	-20.35	-13.86	-12.38	0	1.15

TABLE IV: Performance improvement in percent achieved by Approach B at nominal speed $\omega = 1$ and using the switching horizon 'SSE'. The original MPDBC version is used as a baseline.

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