

# Computationally Efficient Multistep Model Predictive Control for Multilevel Converters

Alberic Benjamin

*School of Electrical and Data Engineering*  
*University of Technology Sydney*  
Sydney, Australia  
alberic.benjamin@uts.edu.au

Pablo Poblete

*School of Electrical and Data Engineering*  
*University of Technology Sydney*  
Sydney, Australia  
pmpoblete@ieee.org

Majid Farhangi

*School of Electrical Engineering and Telecommunication*  
*University of New South Wales*  
Sydney, Australia  
majid.farhangi@ieee.org

Rodrigo H. Cuzmar

*School of Electrical and Data Engineering*  
*University of Technology Sydney*  
Sydney, Australia  
rodrigo.cuzmar@uts.edu.au

George Papafotiou

*Electrical Engineering*  
*Eindhoven University of Technology*  
Eindhoven, Netherlands  
g.papafotiou@tue.nl

Tobias Geyer

*Medium Voltage Drives*  
*ABB System Drives*  
Turgi, Switzerland  
t.geyer@ieee.org

Ricardo P. Aguilera

*School of Electrical and Data Engineering*  
*University of Technology Sydney*  
Sydney, Australia  
raguilera@ieee.org

**Abstract**—Recently, multistep direct model predictive control (MPC) has emerged as an effective control alternative for low-switching high-power converters. These multistep MPC approaches often rely on the Sphere Decoding Algorithm (SDA) to effectively solve the associated optimization process. However, as analyzed in this work, the computational effort required by the SDA-based optimization grows significantly with the number of available output voltage levels in the converter. To address this issue, the work at hand proposes a computationally efficient multistep MPC strategy for multilevel converters. The key idea is to reformulate the converter dynamic model by considering voltage level changes as control inputs, instead of actual voltage levels. This reformulation enables the SDA to search over a finite and reduced set of possible transitions, yielding execution times that are independent of the converter’s voltage levels. Simulation results for a three-phase, 7-level converter are provided to validate the proposed multistep MPC for multilevel converters.

**Index Terms**—Optimal Control, Multilevel Converters, Computational Burden

## I. INTRODUCTION

Finite control set model predictive control (FCS-MPC) has become an promising method for controlling power electronic converters [1]–[4]. Among the main advantages of FCS-MPC are its intuitive formulation and its direct consideration of switching states for semiconductors or voltage levels, eliminating the need for separate modulation stages [5], [6]. FCS-MPC is a multi-variable control strategy and the ability to incorporate constraints, enhancing its flexibility for power electronics applications. Furthermore, the power conversion efficiency can be managed through discouraging power switch commutations. This is achieved by penalizing switching transitions in the

cost function. Due to the lack of a modulator, this approach inherently results in a variable switching frequency that can impact the power quality.

Recently, several multistep or long prediction horizon (LPH) FCS-MPC strategies have been proposed the power quality of the converter while keeping a reduced number of power switch commutations [2]. However, the computational burden required to perform an exhaustive search among all possible switching combinations to select the optimal solution increases exponentially as the prediction horizon is increased [7], [8]. To address this, sphere decoding algorithms (SDAs) have been used to reduce the computational burden to obtain the optimal solution [9]. In essence, this is achieved by solving an integer least-squares (ILS) optimization problem. Here, an initial sphere is formed by considering the unconstrained optimal solution as the center. Then, an initial switch combination is selected as a candidate solution. Thus, the size of this initial sphere is given by the distance from the center to this initial candidate. Then, any switch combination that lies outside the sphere is quickly discarded by the SDA. On the other hand, if the SDA finds a switch combination that lies inside the sphere, then this incumbent solution is used to form a new sphere with a reduced radius. This process is repeated until the sphere cannot be further reduced in size. Consequently, solving the ILS optimization problem is equivalent to determining the switch combination that yields the smallest sphere. Improvements to SDAs have been investigated thoroughly in [10]–[14].

For medium-voltage/high-power applications, multilevel converters provide a reduced total harmonic distortion (THD),

since the converter can generate a staircase voltage that closely resembles a sinusoidal waveform [15]. The main multilevel topologies include the cascaded H-bridge (CHB), modular multilevel converter (MMC), neutral-point clamped (NPC), and Flying Capacitor (FC) [16]–[22]. For multilevel converters, LPH-FCS-MPC also offers THD improvements while operating at low-switching frequency [16], [23].

Despite the improvements in computation times provided by SDA compared to the conventional exhaustive search, the computational burden of LPH-FCS-MPC as the number of converter voltage levels varies has not been explored. Furthermore, if the SDA is not formulated to directly satisfy the unity voltage level switching constraint, post-optimization verification is required, increasing the computational burden. Consequently, the real-time implementation of LPH-FCS-MPC strategies becomes unpredictable for multilevel converters with a large number of output voltage levels.

This paper proposes a computationally efficient multistep MPC strategy that decouples the computational burden of the optimal search from the number of converter levels. The novelty of the proposed strategy lies in reformulating the converter dynamic model to consider voltage level transitions as control inputs, rather than the actual output voltage level. Subsequently, the defined control set for the output voltage transitions per phase is reduced to three alternatives at each sampling instant, significantly reducing the computational burden of SDA and ensuring that the unity voltage level switching constraint is directly satisfied.

## II. PROPOSED INCREMENTAL DYNAMIC MODEL FOR MULTILEVEL CONVERTERS

The generalized model of the 3-phase grid-connected inverter is illustrated in Fig. 1. The states are modeled in the alpha-beta domain for the current,  $i_{\alpha\beta}$ , inverter voltage,  $v_{i,\alpha\beta}$ , and grid voltage  $v_{g,\alpha\beta}$ . Whereas the control input,  $\mathbf{u}_{abc}$ , retains the traditional abc domain. The inverter is connected to the inverter via an inductive filter which has inductance,  $\ell$ , and resistance,  $r$ .

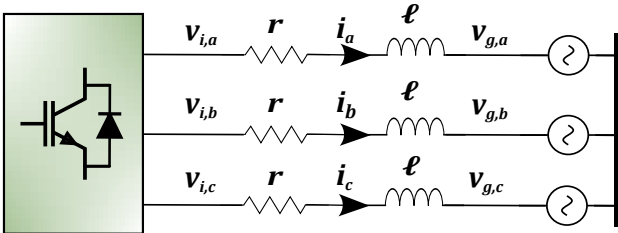


Fig. 1: Grid-connected multilevel converter

The dynamic model for this multilevel converter model is given by:

$$\frac{di_{\alpha}(t)}{dt} = -\frac{r}{\ell}i_{\alpha}(t) + \frac{1}{\ell}v_{i,\alpha}(t) - \frac{1}{\ell}v_{g,\alpha}(t) \quad (1a)$$

$$\frac{di_{\beta}(t)}{dt} = -\frac{r}{\ell}i_{\beta}(t) + \frac{1}{\ell}v_{i,\beta}(t) - \frac{1}{\ell}v_{g,\beta}(t) \quad (1b)$$

$$\frac{dv_{g,\alpha}(t)}{dt} = -\omega v_{g,\beta}(t) \quad (1c)$$

$$\frac{dv_{g,\beta}(t)}{dt} = \omega v_{g,\alpha}(t) \quad (1d)$$

where the Clarke transform,  $\Gamma$ , is applied to translate electrical variables from the  $abc$ - to  $\alpha\beta$ -framework:

$$\mathbf{i}_{\alpha\beta}(t) = \Gamma \mathbf{i}_{abc}(t) \quad (2a)$$

$$\mathbf{v}_{g,\alpha\beta}(t) = \Gamma \mathbf{v}_{g,abc}(t) \quad (2b)$$

$$\mathbf{v}_{i,\alpha\beta}(t) = \Gamma \mathbf{v}_{i,abc}(t) \quad (2c)$$

where

$$\mathbf{v}_{i,abc}(t) = v_{dc} \mathbf{u}_{abc}(t) \quad (3)$$

Accordingly, a three-phase power converter with  $2\eta + 1$  voltage levels has the following FCS of output voltages, which increases exponentially with the number of levels:

$$\mathbf{u}_{abc}(t) \in \mathbf{U} \triangleq \{-\eta, \dots, -1, 0, 1, \dots, \eta\}^3. \quad (4)$$

### A. Continuous-Time Dynamic Model of a Grid-Connected Multilevel Converter

Given that the continuous-time state-space model can be defined as:

$$\dot{\mathbf{x}}(t) = \mathbf{A}_c \mathbf{x}(t) + \mathbf{B}_c \mathbf{u}(t) \quad (5a)$$

$$\mathbf{y}(t) = \mathbf{C}_c \mathbf{x}(t) \quad (5b)$$

where the state, input, and output matrices are:

$$\mathbf{x}(t) = [i_{\alpha}(t) \quad i_{\beta}(t) \quad v_{g,\alpha}(t) \quad v_{g,\beta}(t)]^T \quad (6a)$$

$$\mathbf{y}(t) = [i_{\alpha}(t) \quad i_{\beta}(t)]^T \quad (6b)$$

$$\mathbf{u}(t) = [u_a(t) \quad u_b(t) \quad u_c(t)]^T \quad (6c)$$

Therefore, the state-space matrices are given by:

$$\mathbf{A}_c = \begin{bmatrix} -\frac{r}{\ell} & 0 & -\frac{1}{\ell} & 0 \\ 0 & -\frac{r}{\ell} & 0 & -\frac{1}{\ell} \\ 0 & 0 & 0 & -\omega \\ 0 & 0 & \omega & 0 \end{bmatrix} \quad (7)$$

$$\mathbf{B}_c = \frac{2v_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$\mathbf{C}_c = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}$$

### B. Standard Discrete-Time Dynamic Model of a Multilevel Power Converter

The general discrete-time state-space model defined is defined as:

$$\mathbf{x}(k+1) = \mathbf{A}\mathbf{x}(k) + \mathbf{B}\mathbf{u}(k) \quad (8a)$$

$$\mathbf{y}(k) = \mathbf{C}\mathbf{x}(k) \quad (8b)$$

where the discrete-time state space matrices were determined by applying zero-order hold estimation with sampling time,  $T_s$ :

$$\mathbf{A} = \begin{bmatrix} 1 - \frac{rT_s}{\ell} & 0 & -\frac{T_s}{\ell} & 0 \\ 0 & 1 - \frac{rT_s}{\ell} & 0 & -\frac{T_s}{\ell} \\ 0 & 0 & 1 & -\omega T_s \\ 0 & 0 & \omega T_s & 1 \end{bmatrix} \quad (9)$$

$$\mathbf{B} = \frac{2v_{dc}T_s}{3} \begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}$$

### C. Proposed Incremental Voltage Level-Based System Model

This section presents the proposed incremental voltage level-based system model, which enables decoupling the computational complexity of LPH-FCS-MPC from the number of voltage levels in the converter. The proposed model is motivated by the following factors:

- To limit the  $dv/dt$  applied to the output filter via a unity commutation level constraint [4].
- FCS-MPC strategies often include a term in their cost functions to penalize voltage level transitions,  $\Delta\mathbf{u}$ , and to reduce the average commutation frequency accordingly.

These factors are exploited by the proposed model by rearranging (9) to explicitly consider the voltage level transitions,  $\Delta\mathbf{u}(k) \in \Delta\mathbf{U} \triangleq \{-1, 0, 1\}^3$ , as the control input of the prediction model [24], i.e.:

$$\begin{bmatrix} \mathbf{x}(k+1) \\ \mathbf{u}(k) \end{bmatrix} = \underbrace{\begin{bmatrix} \mathbf{A} & \mathbf{B} \\ 0 & \mathbf{I}_3 \end{bmatrix}}_{\mathbf{A}_z} \begin{bmatrix} \mathbf{x}(k) \\ \mathbf{u}(k-1) \end{bmatrix} + \underbrace{\begin{bmatrix} \mathbf{B} \\ \mathbf{I}_3 \end{bmatrix}}_{\mathbf{B}_z} \Delta\mathbf{u}(k) \quad (10a)$$

$$\mathbf{y}(k) = \underbrace{\begin{bmatrix} \mathbf{C} & 0 \end{bmatrix}}_{\mathbf{C}_z} \mathbf{z}(k) \quad (10b)$$

where

$$\Delta\mathbf{u}(k) = \mathbf{u}(k) - \mathbf{u}(k-1) \quad (11a)$$

$$\mathbf{z}(k) = [\mathbf{x}^T(k) \quad \mathbf{u}^T(k-1)]^T \quad (11b)$$

Finally, using (11), the augmented state-space equation becomes:

$$\mathbf{z}(k+1) = \mathbf{A}_z\mathbf{z}(k) + \mathbf{B}_z\Delta\mathbf{u}(k) \quad (12)$$

### III. PROPOSED MULTISTEP MPC FORMULATION

The standard multistep MPC cost function for a prediction horizon  $N$  is given by [6]:

$$J(k) = \sum_{\ell=k}^{k+N-1} \|\mathbf{y}_e(\ell+1)\|_2^2 + \sigma \|\Delta\mathbf{u}(\ell)\|_2^2 \quad (13)$$

where the output error,  $\mathbf{y}_e(k)$ , is expanded based on the measured output,  $\mathbf{y}(k)$ , and reference output,  $\mathbf{y}^*(k)$ :

$$\mathbf{y}_e(k) = \mathbf{y}(k) - \mathbf{y}^*(k). \quad (14)$$

In this work, the constrained optimal control problem is formulated as:

$$\Delta\mathbf{U}(k)^{\text{opt}} = \arg \min_{\Delta\mathbf{U}(k)} J(k); \quad (15)$$

$$\text{s.t. } \Delta\mathbf{U}(k) \in \Delta\mathbf{U}^N \quad (\text{FCS constraint}) \quad (16a)$$

$$\|\Delta\mathbf{u}(k)\|_\infty \leq 1 \quad (\text{Unity level transition}) \quad (16b)$$

$$\mathbf{u}_{\min} \leq \mathbf{u}(k) \leq \mathbf{u}_{\max} \quad (\text{Voltage level bound}). \quad (16c)$$

where

$$\mathbf{u}_{\max} = [\eta \quad \eta \quad \eta]^T \quad (17)$$

$$\mathbf{u}_{\min} = -[\eta \quad \eta \quad \eta]^T$$

#### A. Proposed incremental optimization problem

In comparison to the conventional set of voltage levels  $\mathbf{U}$ , the FCS  $\Delta\mathbf{U}$  used by the proposed model is fixed and independent of the voltage level number. As a consequence, it is possible to derive the following long-horizon prediction model in terms of future voltage incremental level transitions:

$$\mathbf{Z}(k+1) = \mathbf{\Lambda}_z\mathbf{z}(k) + \mathbf{\Phi}_z\Delta\mathbf{U}(k) \quad (18)$$

$$\mathbf{Y}(k+1) = \mathbf{C}\mathbf{Z}(k+1),$$

where the state-space matrices over the prediction given prediction horizon are:

$$\mathbf{Z}(k+1) = [\mathbf{z}^T(k+1) \quad \dots \quad \mathbf{z}^T(k+N+1)]^T \quad (19a)$$

$$\mathbf{Y}(k+1) = [\mathbf{y}^T(k+1) \quad \dots \quad \mathbf{y}^T(k+N+1)]^T \quad (19b)$$

$$\Delta\mathbf{U}(k) = [\Delta\mathbf{u}^T(k) \quad \dots \quad \Delta\mathbf{u}^T(k+N)]^T \quad (19c)$$

The matrices  $\mathbf{\Lambda}_z$ ,  $\mathbf{\Phi}_z$ , and  $\mathbf{C}$  can be obtain following the standard procedure in presented in [6]:

$$\mathbf{\Phi}_z = \begin{bmatrix} \mathbf{C}_z\mathbf{B}_z & \mathbf{0} & \dots & \mathbf{0} \\ \mathbf{C}_z\mathbf{A}_z\mathbf{B}_z & \mathbf{C}_z\mathbf{B}_z & \dots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{C}_z\mathbf{A}_z^{N-1}\mathbf{B}_z & \mathbf{C}_z\mathbf{A}_z^{N-2}\mathbf{B}_z & \dots & \mathbf{C}_z\mathbf{B}_z \end{bmatrix} \quad (20)$$

$$\mathbf{\Lambda}_z = \begin{bmatrix} \mathbf{C}_z\mathbf{A}_z \\ \mathbf{C}_z\mathbf{A}_z^2 \\ \vdots \\ \mathbf{C}_z\mathbf{A}_z^N \end{bmatrix}$$

Considering the prediction model (18), the cost function (13) can be re-written as a convex quadratic function:

$$J(k) = \Delta\mathbf{U}(k)^T \mathbf{W}_z \Delta\mathbf{U}(k) + 2\Delta\mathbf{U}^T(k) \mathbf{F}_z(k) \quad (21)$$

where

$$\mathbf{W}_z = \Phi_z^T \Phi_z + \sigma \mathbf{I}_N \quad (22a)$$

$$\mathbf{F}_z(k) = \Phi_z^T (\Lambda_z \mathbf{z}(k) - \mathbf{Y}_N^*). \quad (22b)$$

### B. System Constraints

Constraints are applied to select an optimal solution that meets the unity transition limit and the number of converter voltage levels. The model constraints applied to the control response are derived from (16b) and (16c). The expansion of the constraints for quadratic programming (QP) formulation over the prediction horizon defined in terms of  $\Delta \mathbf{u}$  is [25]:

$$\mathbf{C}_2 \Delta \mathbf{U}(k) \preceq \mathbf{U}_{max}(k) - \mathbf{C}_1 \mathbf{u}(k-1) \quad (23a)$$

$$-\mathbf{C}_2 \Delta \mathbf{U}(k) \preceq \mathbf{U}_{min}(k) + \mathbf{C}_1 \mathbf{u}(k-1) \quad (23b)$$

$$\Delta \mathbf{U}(k) \preceq \Delta \mathbf{U}_{max}(k) \quad (23c)$$

$$-\Delta \mathbf{U}(k) \preceq \Delta \mathbf{U}_{min}(k) \quad (23d)$$

where the constraint matrices are defined:

$$\mathbf{U}_{max}(k) = [\mathbf{u}_{max}^T(k) \quad \cdots \quad \mathbf{u}_{max}^T(k+N)]^T \quad (24a)$$

$$\mathbf{U}_{min}(k) = [\mathbf{u}_{min}^T(k) \quad \cdots \quad \mathbf{u}_{min}^T(k+N)]^T \quad (24b)$$

$$\mathbf{C}_1 = \begin{bmatrix} \mathbf{I} \\ \mathbf{I} \\ \vdots \\ \mathbf{I} \end{bmatrix}, \quad \mathbf{C}_2 = \begin{bmatrix} \mathbf{I} & 0 & \cdots & 0 \\ \mathbf{I} & \mathbf{I} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{I} & \mathbf{I} & \cdots & \mathbf{I} \end{bmatrix} \quad (25)$$

### C. Proposed SDA for $\Delta \mathbf{U}$

In this work, it is proposed to obtain the sphere center by solving the following constrained QP problem:

$$\begin{aligned} \Delta \mathbf{U}_{qp}^{opt}(k) &= \arg \min_{\Delta \mathbf{U}(k)} J(k); \\ \text{s.t. } & (16b)-(16c). \end{aligned} \quad (26)$$

The constraint in (16a) is used to formulate the SDA where  $\Theta(k) = \mathbf{H}_\Delta \Delta \mathbf{U}_{qp}^{opt}(k)$  is considered the sphere centre:

$$\Delta \mathbf{U}^{opt}(k) = \arg \left\{ \min_{\Delta \mathbf{U}(k)} \|\mathbf{H}_\Delta \Delta \mathbf{U}(k) - \Theta(k)\|_2^2 \right\} \quad (27)$$

where  $\mathbf{H}_\Delta$  is a triangular matrix that is found using the Cholesky decomposition of  $\mathbf{W}_z = \mathbf{H}_\Delta^T \mathbf{H}_\Delta$ . To maintain a small initial sphere during transients, the initial control input,  $\Delta \mathbf{U}_{ini}$ , is obtained by quantizing each vector  $\Delta \mathbf{u}_{qp}$  in  $\Delta \mathbf{U}_{qp}$  to the nearest discrete level while satisfying the voltage constraint in (17) [17].

The SDA initial sphere radius,  $\rho_{ini}$ , in terms of  $\Delta \mathbf{u}$  in (28).

$$\rho_{ini}^2 = \|\mathbf{H}_\Delta \Delta \mathbf{U}_{ini} - \Theta\|_2^2 \quad (28)$$

The SDA will use Time Ascending Order search strategy with a lower triangular  $\mathbf{H}_\Delta$  matrix. A breakdown of the implemented algorithm is shown in Algorithm 1. The search levels variable,  $p = 3N$ . Finally, the optimal input voltage sequence selected by the SDA is expanded in (29)

$$\Delta \mathbf{U}^{opt}(k) = [(\Delta \mathbf{u}^{opt}(k))^T \quad \cdots \quad (\Delta \mathbf{u}^{opt}(k+N))^T]^T \quad (29)$$

$$\mathbf{u}^{opt}(k) = \Delta \mathbf{u}^{opt}(k) + \mathbf{u}(k-1). \quad (30)$$

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### Algorithm 1 Incremental SDA

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**Require:**  $\Delta \mathbf{U}_{ini}$ : Initial solution,

1:  $\mathbf{H}_\Delta$ : Transformation matrix,

2:  $p$ : Search levels,

3:  $\Theta$ : Sphere center

**Ensure:**  $\Delta \mathbf{U}^{opt}$ : ILS optimal solution

4:  $\rho_{inc} \leftarrow \rho_{ini}$

5:  $k_c \leftarrow 0$

6:  $i \leftarrow 1$

7: **while**  $i > 0$  **do**

8:    $\Delta \mathbf{u}_i \leftarrow k_c - 1$

9:   **if**  $\Delta \mathbf{u}_i > 1$  **then**

10:      $i \leftarrow i - 1$

11:     **if**  $i > 0$  **then**

12:        $k_c \leftarrow \Delta \mathbf{U}_i + 2$

13:     **end if**

14:     **continue**

15:   **end if**

16:    $\Delta \mathbf{U}_{[1:i]} \leftarrow \Delta \mathbf{u}_i$

17:    $\rho_i^2 \leftarrow \|\mathbf{H}_{\Delta[i,1:i]} \Delta \mathbf{U}_{[1:i]} - \Theta_i\|_2^2 + \rho_{i-1}^2$

18:   **if**  $\rho_i > \rho_{inc}$  **then**

19:      $k_c \leftarrow k_c + 1$

20:     **continue**

21:   **end if**

22:   **if**  $\rho_i \leq \rho_{inc}$  **then**

23:     **if**  $i == p$  **then**

24:        $\Delta \mathbf{U}^{opt} \leftarrow \Delta \mathbf{U}$

25:        $\rho_{inc} \leftarrow \rho_p$

26:        $k_c \leftarrow k_c + 1$

27:     **else**

28:        $i \leftarrow i + 1$

29:        $k_c \leftarrow 0$

30:     **end if**

31:   **end if**

32: **end while**

33: **return**  $\mathbf{U}^{opt}$

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## IV. SIMULATION RESULTS

Simulations of a 3-phase grid-connected CHB converter were conducted to evaluate the closed-loop performance of the proposed incremental multistep ( $\Delta \mathbf{u}$ -MPC) in comparison to the standard multistep (u-MPC). The prediction horizon was set with  $N = 4$  for both  $\Delta \mathbf{u}$ -MPC and u-MPC methods. The sampling frequency was 10kHz, and the  $\sigma$  factor was tuned for each formulation to achieve a 1.8 kHz switching frequency. To evaluate the execution time, THD, and current error tracking, the number of levels,  $n_L$ , simulated is varied from 3 to 11. The isolated DC-bus voltage for each CHB cell is varied with  $n_L$ , so the sum of all the voltages is 720 VDC. Enabling a constant current reference across all levels.

A closed-loop dynamic result of the transient performance of the 7-level CHB for the proposed method is shown in Fig. 2a. It is evident that the proposed multistep  $\Delta \mathbf{u}$ -MPC exhibits both a fast dynamic response and competitive steady-

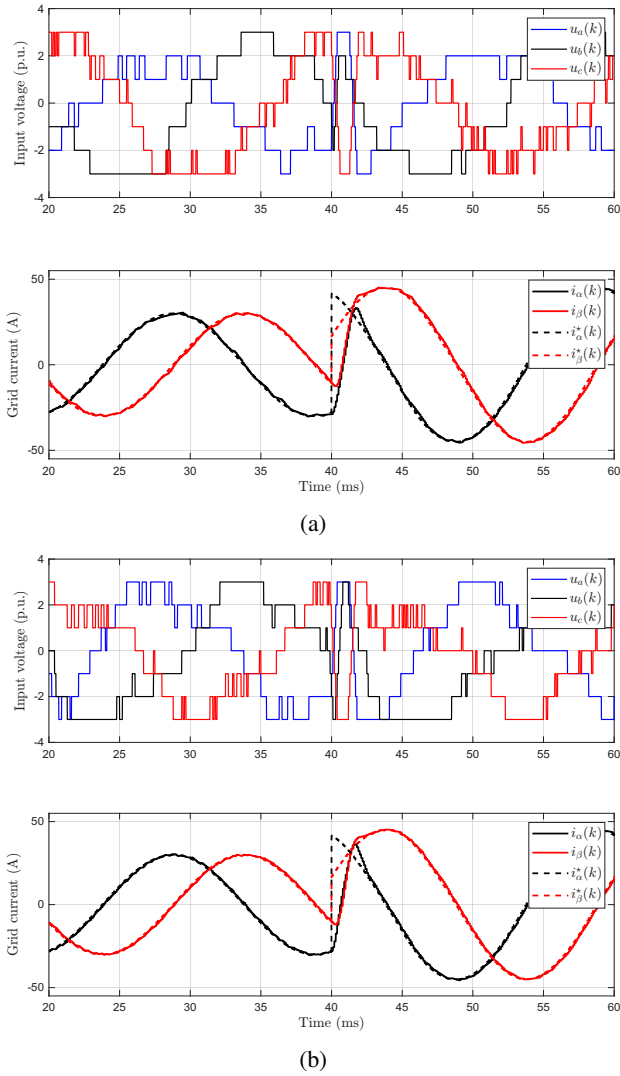


Fig. 2: Simulated closed-loop response: a) Proposed multistep  $\Delta u$ -MPC; b) standard multistep  $u$ -MPC.

state performance. Additionally, this proposal is compared with the standard multistep  $u$ -MPC [17] in Fig. 2b. Here, it can be observed that both present a similar closed-loop response in terms of the current tracking. Note that the switching voltages for the proposed multistep  $\Delta u$ -MPC appear to be less symmetrical than the standard multistep MPC.

The  $\text{THD}_i$  and average tracking error were selected as metrics to evaluate the power quality performance of both formulations. The performance of these metrics in relation to  $n_L$  indicates a consistent advantage of the standard formulation. The  $\text{THD}_i$  and target tracking performance as  $n_L$  varies for the two formulations are tabulated in Table. I. Both these metrics indicate that the standard formulation has better power quality performance. As the levels increase from 3 to 7, the  $\text{THD}_i$  variation between the two methods decreases drastically. The ratio of variation in the  $\text{THD}_i$  difference between 7 levels and 9 levels is marginal. As the converter levels vary, the average current tracking error is consistently lower in

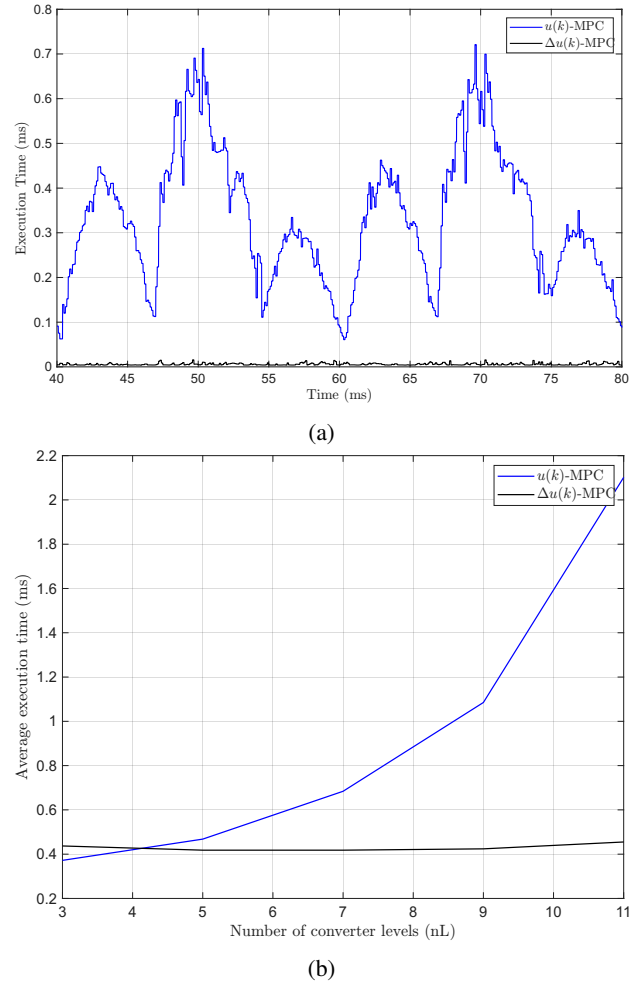


Fig. 3: Computational burden; a) Execution time for  $n_L = 7$ ; b) Average execution time for different voltage levels.

TABLE I: Variation of current quality with  $n_L$  for  $N = 4$

	THD <sub>i</sub> (%)		Tracking Error (%)	
	$u$ -MPC	$\Delta u$ -MPC	$u$ -MPC	$\Delta u$ -MPC
3	3.89	5.85	3.74	4.12
5	1.84	2.33	3.53	3.58
7	1.45	1.64	3.43	3.42
9	0.96	1.11	2.72	2.82
11	0.74	0.9	2.16	2.5

the standard method. However, the difference is marginal for levels 3 to 9. The standard method demonstrates improved power quality compared to the proposed  $\Delta u$  method across the assessed range of incremental voltage levels. This is likely a result of the larger search space of the SDA for the standard methodology, which relates the available voltage levels directly to the reference current.

Although the proposed strategy has a disadvantage from a power quality perspective, the main benefit of this proposal lies in the reduced computational burden, as illustrated in Fig. 3a. Additionally, Fig. 3b shows the required average execution time for both multistep strategies as the voltage

TABLE II: Execution time comparison by computation stage for  $N = 4$

Levels	$u$ -MPC		$\Delta u$ -MPC	
	QP (ms)	SDA (ms)	QP (ms)	SDA (ms)
3	0.347	0.025	0.428	0.009
5	0.348	0.120	0.404	0.014
7	0.399	0.285	0.403	0.015
9	0.366	0.719	0.409	0.015
11	0.392	1.7	0.437	0.018

levels increase. The incremental  $\Delta u$ -MPC method retains consistent computation independent of the number of voltage levels. In contrast, the  $u$ -MPC average execution time is only comparable for a 3-level case. Then, it exponentially increases as the voltage level increases, showing that the proposed  $\Delta u$ -MPC is better suited for multilevel converters with more than three levels. Notably, the  $n_L$  influence on the computation time for the  $u$ -MPC may lead to suboptimal implementation of higher levels. Arguably, this will increase the THD<sub>i</sub> for the  $u$ -MPC with higher  $n_L$ .

Separating the execution time into the two major optimization components provides further insight into the computational advantage of the proposed formulation. The two optimization stages are the preconditioning stage, which selects the initial sphere center using a QP solver, and the SDA optimal solution search. The tabulation of the two computational stages average execution time is shown in Table II. These results demonstrate that the proposed  $\Delta u$  formulation is computationally advantageous in the SDA search stage. Whereas the additional constraints on the QP preconditioning demonstrate an increased computation time. Referring back to Fig. 3b, the increased computational time of the proposed  $\Delta u$  formulation illustrates a disadvantage for a 3-level CHB. Nonetheless, the proposed  $\Delta u$  formulation indicates a relatively consistent SDA pre-conditioning and search time compared to the standard formulation. This is likely a direct result of the number of possible incremental voltage levels being searched at each cycle remaining constant regardless of  $n_L$ .

## V. CONCLUSION AND FUTURE WORK

In this paper, a computationally efficient multistep MPC suitable for multilevel converters has been proposed. The proposed strategy is based on an intuitive reformulation of the converter model, which decouples the computational complexity of the SDA solver from the number of converter levels.

Simulation results are provided to assess the performance of the proposed strategy against a standard multistep MPC strategy. These results demonstrate that the proposed strategy exhibits transient and steady-state performance comparable to that of the standard multistep MPC, albeit with a marginal disadvantage in terms of power quality. Nevertheless, the execution time is drastically reduced, enabling the implementation of this strategy for converters with a larger number of cells.

Future work will primarily focus on enabling this system in a prototype converter to evaluate the real-time feasibility

of the system. Experimentation and analysis on improving the power quality whilst managing execution time will be explored. Finally, future work will experiment on reducing switching losses and asymmetry.

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